MU183020A
28G/32G bit/s PPG
MU183021A
28G/32G bit/s 4ch PPG
Operation Manual

14th Edition

- **For safety and warning information, please read this manual before attempting to use the equipment.**
- **Additional safety and warning information is provided in the MP1800A Signal Quality Analyzer Installation Guide and the MT1810A 4 Slot Chassis Installation Guide. Please also refer to one of these documents before using the equipment.**
- **Keep this manual with the equipment.**

ANRITSU CORPORATION

Document No.: M-W3594AE-14.0

Safety Symbols

To prevent the risk of personal injury or loss related to equipment malfunction, Anritsu Corporation uses the following safety symbols to indicate safety-related information. Ensure that you clearly understand the meanings of the symbols BEFORE using the equipment. Some or all of the following symbols may be used on all Anritsu equipment. In addition, there may be other labels attached to products that are not shown in the diagrams in this manual.

Symbols used in manual

⚠ DANGER This indicates a very dangerous procedure that could result in serious injury or death if not performed properly.

⚠ WARNING This indicates a hazardous procedure that could result in serious injury or death if not performed properly.

⚠ CAUTION This indicates a hazardous procedure or danger that could result in light-to-severe injury, or loss related to equipment malfunction, if proper precautions are not taken.

Safety Symbols Used on Equipment and in Manual

The following safety symbols are used inside or on the equipment near operation locations to provide information about safety items and operation precautions. Ensure that you clearly understand the meanings of the symbols and take the necessary precautions BEFORE using the equipment.

This indicates a prohibited operation. The prohibited operation is indicated symbolically in or near the barred circle.

This indicates an obligatory safety precaution. The obligatory operation is indicated symbolically in or near the circle.

This indicates a warning or caution. The contents are indicated symbolically in or near the triangle.

This indicates a note. The contents are described in the box.

These indicate that the marked part should be recycled.

MU183020A 28G/32G bit/s PPG
MU183021A 28G/32G bit/s 4ch PPG
Operation Manual

20 July 2012 (First Edition)
4 April 2016 (14th Edition)

Equipment Certificate

Anritsu Corporation certifies that this equipment was tested before shipment using calibrated measuring instruments with direct traceability to public testing organizations recognized by national research laboratories, including the National Institute of Advanced Industrial Science and Technology, and the National Institute of Information and Communications Technology, and was found to meet the published specifications.

Anritsu Warranty

Anritsu Corporation will repair this equipment free-of-charge if a malfunction occurs within one year after shipment due to a manufacturing fault. However, software fixes will be made in accordance with the separate Software End-User License Agreement. Moreover, Anritsu Corporation will deem this warranty void when:

- The fault is outside the scope of the warranty conditions separately described in the operation manual.
- The fault is due to mishandling, misuse, or unauthorized modification or repair of the equipment by the customer.
- The fault is due to severe usage clearly exceeding normal usage.
- The fault is due to improper or insufficient maintenance by the customer.
- The fault is due to natural disaster, including fire, wind, flooding, earthquake, lightning strike, or volcanic ash, etc.
- The fault is due to damage caused by acts of destruction, including civil disturbance, riot, or war, etc.
- The fault is due to explosion, accident, or breakdown of any other machinery, facility, or plant, etc.
- The fault is due to use of non-specified peripheral or applied equipment or parts, or consumables, etc.
- The fault is due to use of a non-specified power supply or in a non-specified installation location.
- The fault is due to use in unusual environments(Note).
- The fault is due to activities or ingress of living organisms, such as insects, spiders, fungus, pollen, or seeds.

In addition, this warranty is valid only for the original equipment purchaser. It is not transferable if the equipment is resold.

Anritsu Corporation shall assume no liability for injury or financial loss of the customer due to the use of or a failure to be able to use this equipment.

Note:
For the purpose of this Warranty, "unusual environment" means use:

- In places of direct sunlight
- In dusty places
- Outdoors
- In liquids, such as water, oil, or organic solvents, and medical fluids, or places where these liquids may adhere
- In salty air or in place chemically active gases (sulfur dioxide, hydrogen sulfide, chlorine, ammonia, nitrogen dioxide, or hydrogen chloride etc.) are present
- In places where high-intensity static electric charges or electromagnetic fields are present
- In places where abnormal power voltages (high or low) or instantaneous power failures occur
- In places where condensation occurs
- In the presence of lubricating oil mists
- In places at an altitude of more than 2,000 m
- In the presence of frequent vibration or mechanical shock, such as in cars, ships, or airplanes

Anritsu Corporation Contact

In the event of this equipment malfunctions, contact an Anritsu Service and Sales office. Contact information can be found on the last page of the printed version of this manual, and is available in a separate file on the CD version.

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This product and its manuals may require an Export License/Approval by the Government of the product's country of origin for re-export from your country.

Before re-exporting the product or manuals, please contact us to confirm whether they are export-controlled items or not.

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   ii) If this Software is used in conjunction with other non-Anritsu-approved software.
   iii) Recovery of lost or damaged data.
   iv) If this Software or the Equipment has been modified, repaired, or otherwise altered without Anritsu's prior approval.
   v) For any other reasons out of Anritsu's direct control and responsibility, such as but not limited to, natural disasters, software virus infections, etc.

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Anritsu shall deem this EULA terminated if you violate any conditions described herein. This EULA shall also be terminated if the conditions herein cannot be continued for any good reason, such as violation of copyrights, patents, or other laws and ordinances.

6. Reparations

If Anritsu suffers any loss, financial or otherwise, due to your violation of the terms of this EULA, Anritsu shall have the right to seek proportional damages from you.

7. Responsibility after Termination

Upon termination of this EULA in accordance with item 5, you shall cease all use of this Software immediately and shall as directed by Anritsu either destroy or return this Software and any backup copies, full or partial, to Anritsu.

8. Dispute Resolution

If matters of dispute or items not covered by this EULA arise, they shall be resolved by negotiations in good faith between you and Anritsu.

9. Court of Jurisdiction

This EULA shall be interpreted in accordance with Japanese law and any disputes that cannot be resolved by negotiation described in Article 8 shall be settled by the Japanese courts.

CE Conformity Marking

Anritsu affixes the CE Conformity marking on the following product(s) in accordance with the Council Directive 93/68/EEC to indicate that they conform to the EMC and LVD directive of the European Union (EU).

CE marking

1. Product Model

Plug-in Units: MU183020A 28G/32G bit/s PPG
MU183021A 28G/32G bit/s 4ch PPG

2. Applied Directive and Standards

When the MU183020A 28G/32G bit/s PPG or MU183021A 28G/32G bit/s 4ch PPG is installed in the MP1800A or MT1810A, the applied directive and standards of this unit conform to those of the MP1800A or MT1810A main frame.

PS: About main frame
Please contact Anritsu for the latest information on the main frame types that MU183020A / MU183021A can be used with.

C-Tick Conformity Marking

Anritsu affixes the C-tick marking on the following product(s) in accordance with the regulation to indicate that they conform to the EMC framework of Australia/New Zealand.

C-Tick marking

1. Product Model

Plug-in Units: MU183020A 28G/32G bit/s PPG
MU183021A 28G/32G bit/s 4ch PPG

2. Applied Directive and Standards

When the MU183020A 28G/32G Gbit/s PPG or MU183021A 28G/32G bit/s 4ch PPG is installed in the MP1800A or MT1810A, the applied directive and standards of this unit conform to those of the MP1800A or MT1810A main frame.

PS: About main frame
Please contact Anritsu for the latest information on the main frame types that MU183020A / MU183021A can be used with.

About This Manual

A testing system combining an MP1800A Signal Quality Analyzer or MT1810A 4-Slot Chassis mainframe, module(s), and control software is called a Signal Quality Analyzer Series. The operation manuals of the Signal Quality Analyzer Series consist of separate documents for the installation guide, the mainframe, remote control operation, module(s), and control software, as shown below.

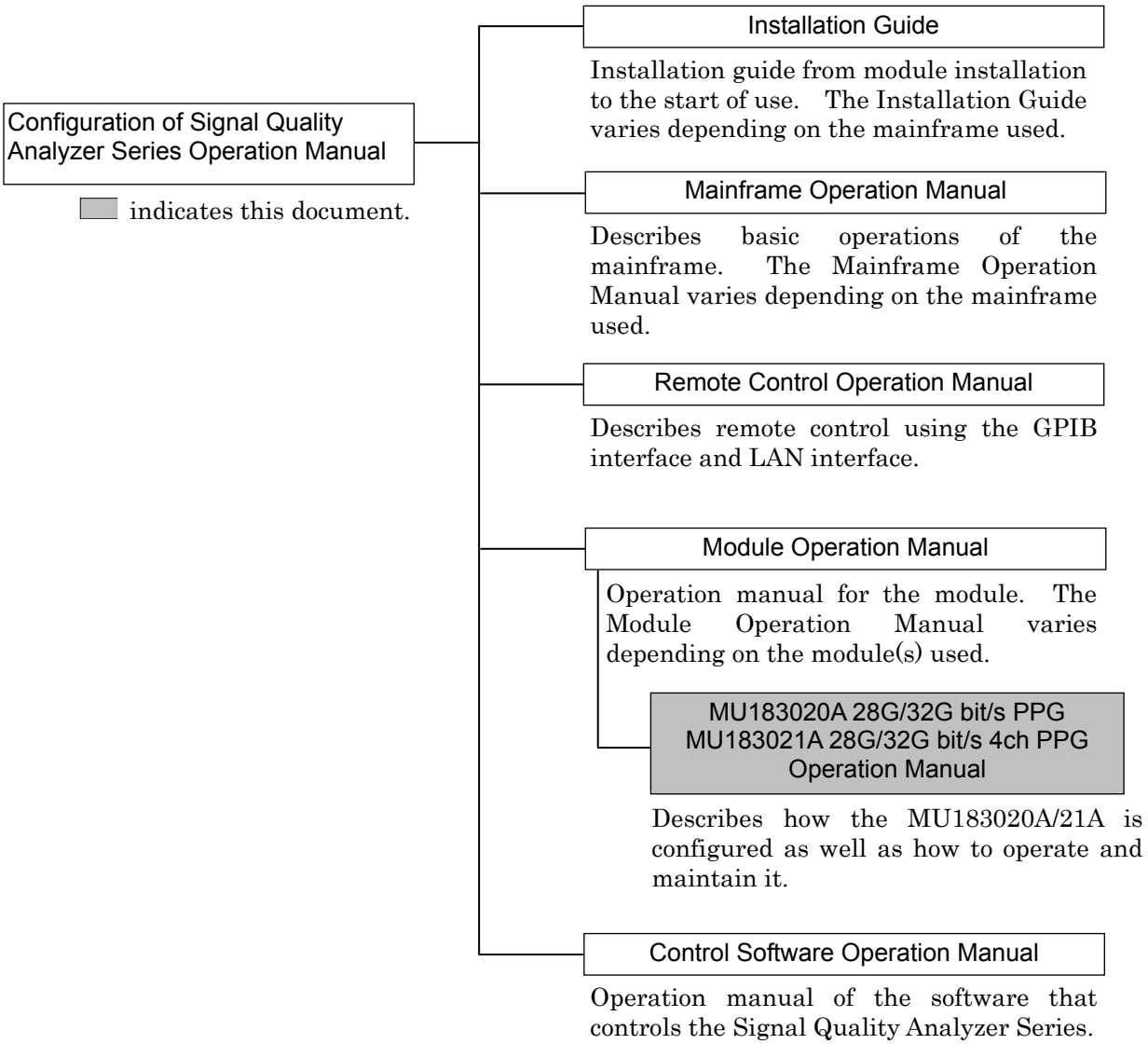


Table of Contents

Chapter 1 Overview

This chapter provides an overview of the MU183020A 28G/32G bit/s PPG and the MU183021A 28G/32G bit/s 4ch PPG (hereinafter, referred to as "MU183020A").
This document only explains the MU183020A, unless there is a special item.

1.1 Product Overview

The MU183020A is a plug-in module that can be built into a Signal Quality Analyzer mainframe.

It can generate a variety of patterns within the operating frequency range, including PRBS, DATA, Zero-Substitution, and Mixed patterns.

Various option configurations are available for the MU183020A. This module is therefore useful for research, development, and production of various types of digital communication equipment, modules, and devices.

The features of this module are listed below:

- Capable of generating PRBS, DATA, Zero-Substitution, and Mixed patterns.
- Capable of outputting while synchronizing multiple-channel signal bits. (Channel Synchronization)
- For MU183020A-x22/x23 and MU183021A, Channel Combination between channels in a module can be performed.
  This enables the generation of multiplexing signal by using Multiplexer (MUX) and De-multiplexer (DEMUX).
- Wide range of output level from 0.5 to 3.5 Vp-p (Option x13/x23)

1.2 Product Composition

1.2.1 Standard configuration

Table 1.2.1-1 and Table 1.2.1-2 show the standard compositions of the MU183020A/MU183021A.

Table 1.2.1-1 Standard composition of MU183020A

Item	Model name/symbol	Product name	Q'ty	Remarks
Mainframe	MU183020A	28G/32G bit/s PPG	1	
Accessories	J0541E	6 dB Fixed Attenuator	1	
	J1137	Terminator	3	Clock Output, Aux Output × 2
	J1359A	Coaxial Adaptor (K-P.K-J,SMA)	1	Clock Output
	J1341A	Open	1	Ext Clock Input
	Z0897A	MP1800A Manual CD	1	CD-ROM
	Z0918A	MX180000A Software CD	1	CD-ROM

Table 1.2.1-2 Standard composition of MU183021A

Item	Model name/symbol	Product name	Q'ty	Remarks
Mainframe	MU183021A	28G/32G bit/s 4ch PPG	1	
Accessories	J0541E	6 dB Fixed Attenuator	1	
	J1137	Terminator	3	Clock Output, Aux Output × 2
	J1359A	Coaxial Adaptor (K-P.K-J,SMA)	1	Clock Output
	J1341A	Open	1	Ext Clock Input
	Z0897A	MP1800A Manual CD	1	CD-ROM
	Z0918A	MX180000A Software CD	1	CD-ROM

1.2.2 Options

Table 1.2.2-1 and Table 1.2.2-2 show the options for the MU183020A/MU183021A. Table 1.2.2-3, Table 1.2.2-4 and Table 1.2.2-5 show the application parts for option. All options are sold separately.

Table 1.2.2-1 Options of MU183020A

Model name	Product name	Remarks
MU183020A-x01	32G bit/s Extension	
MU183020A-x12	1ch 2 V Data Output	*1
MU183020A-x13	1ch 3.5 V Data Output	*1
MU183020A-x22	2ch 2 V Data Output	*1
MU183020A-x23	2ch 3.5 V Data Output	*1
MU183020A-x30	1ch Data Delay	*2
MU183020A-x31	2ch Data Delay	*3

*1: Select one from among them.

*2: The MU183020A-x12/x13 is required.

*3: The MU183020A-x22/x23 is required.

Table 1.2.2-2 Options of MU183021A

Model name	Product name	Remarks
MU183021A-x01	32G bit/s Extension	
MU183021A-x12	4ch 2 V Data Output	*
MU183021A-x13	4ch 3.5 V Data Output	*
MU183021A-x30	4ch Data Delay	

*: Select either of them.

Note:

Option name format is as follows:

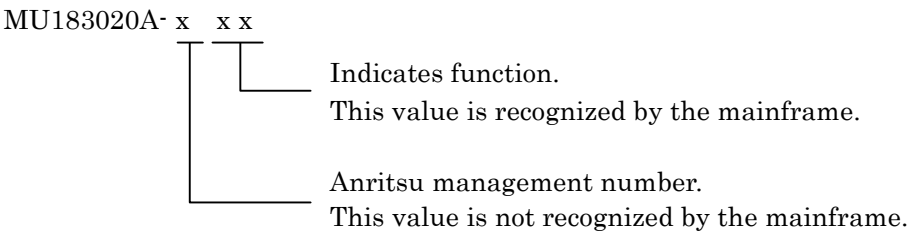


Table 1.2.2-3 Application parts for MU183020A-x12/x13

Model name/symbol	Product name	Q'ty	Remarks
J1137	Terminator	2	Data Output × 2
J1359A	Coaxial Adaptor (K-P.K-J,SMA)	2	Data Output × 2

Table 1.2.2-4 Application parts for MU183020A-x22/x23

Model name/symbol	Product name	Q'ty	Remarks
J1137	Terminator	4	Data Output × 4
J1359A	Coaxial Adaptor (K-P.K-J,SMA)	4	Data Output × 4

Table 1.2.2-5 Application parts for MU183021A-x12/x13

Model name/symbol	Product name	Q'ty	Remarks
J1137	Terminator	8	Data Output × 8
J1359A	Coaxial Adaptor (K-P.K-J,SMA)	8	Data Output × 8

1.2.3 Application parts

Table 1.2.3-1 shows the application parts for the MU183020A. All application parts are sold separately.

Table 1.2.3-1 Application Parts

Model name/ symbol	Product name	Remarks
J1449A	Measurement kit	Coaxial cable (K connector) 0.8 m × 2 Coaxial cable 0.8 m × 2 Coaxial cable 1.0 m × 1
J1343A	Coaxial cable 1 m	SMA connector
J1342A	Coaxial cable 0.8 m	APC3.5 mm connector
J1439A	Coaxial cable (0.8 m, K connector)	K connector
J1137	Terminator	
J1359A	Coaxial Adaptor (K-P.K-J,SMA)	
41KC-3	Precision Fixed Attenuator 3 dB	
41KC-6	Precision Fixed Attenuator 6 dB	
41KC-10	Precision Fixed Attenuator 10 dB	
41KC-20	Precision Fixed Attenuator 20 dB	
K240C	Precision Power Divider	
J1349A	Coaxial Cable 0.3 m	APC3.5 mm connector
J1550A	Coaxial skew match cable (0.8 m, APC3.5 connector)	APC 3.5 mm connector, Pair cable
J1551A	Coaxial skew match cable (0.8 m, K connector)	Pair cable
J1611A	Coaxial cable (1.3 m, K connector)	K connector
J1612A	Fixed Electrical Length Coaxial Cable (0.8 m, K Connector)	K connector
J1615A*	Coaxial Cable set (Jitter-PPG-Emphasis)	Cable set for jitter tolerance measurement
J1618A*	Coaxial Cable set (Jitter-2chPPG-Emphasis)	Cable set for jitter tolerance measurement
J1620A	Coaxial Cable (0.9m K Connector)	K connector
W3594AE	MU183020A/MU183021A Operation manual	Printed version, English
W3594AW	MU183020A/MU183021A Operation manual	Printed version, Japanese
Z0306A	Wrist strap	
MZ1834A	4PAM Converter	
MZ1838A	8PAM Converter	
J1678A	ESD Protection Adapter-K	K connector

*: For examples of how to connect instruments with coaxial cables, refer to Appendix F.

1.3 Specifications

1.3.1 Specifications for MU183020A

Table 1.3.1-1 Operating Bit Rate

Item	Specifications
MU181000A/B synchronized operation ON	This item can be specified when MU181000A or MU181000B are installed to the same unit.
When the Output Clock Rate is set to Full Rate	
Setting Range	2.400 000 to 12.500 000 Gbit/s / 0.000 001 Gbit/s step 12.500 002 to 20.000 000 Gbit/s / 0.000 002 Gbit/s step 20.000 002 to 25.000 000 Gbit/s / 0.000 002 Gbit/s step 25.000 004 to 28.100 000 Gbit/s / 0.000 004 Gbit/s step*1 25.000 004 to 32.100 000 Gbit/s / 0.000 004 Gbit/s step*2
Offset	–1000 to +1000 ppm / 1 ppm step*3
When the Output Clock Rate is set to Half Rate	
Setting Range	2.400 000 to 25.000 000 Gbit/s / 0.000 002 Gbit/s step 25.000 004 to 28.100 000 Gbit/s / 0.000 004 Gbit/s step*1 25.000 004 to 32.100 000 Gbit/s / 0.000 004 Gbit/s step*2
Offset	–1000 to +1000 ppm / 1 ppm step*3

*1: Not available Option x01

*2: Available Option x01

*3: The setting range varies depending on the bit rate setting.
At following bit rate setting, setting range is from –1000 to 0 ppm.

Full rate: 12.500000 Gbit/s, 25.000000 Gbit/s

Half rate: 25.000000 Gbit/s

Table 1.3.1-1 Operating Bit Rate (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>MU181500B synchronized operation ON
When the Output Clock Rate is set to Full Rate
Setting Range

Offset
When the Output Clock Rate is set to Half Rate
Setting Range

Offset</td><td>This item can be specified when MU181000A, MU181000B and MU181500B are installed to the same unit.

2.400 000 to 3.125 000 Gbit/s / 0.000 001 Gbit/s step
3.200 001 to 6.250 000 Gbit/s / 0.000 001 Gbit/s step
6.400 001 to 12.500 000 Gbit/s / 0.000 001 Gbit/s step
12.800 002 to 15.000 000 Gbit/s / 0.000 002 Gbit/s step
15.000 002 to 20.000 000 Gbit/s / 0.000 002 Gbit/s step
20.000 002 to 25.000 000 Gbit/s / 0.000 002 Gbit/s step
25.600 004 to 28.100 000 Gbit/s / 0.000 004 Gbit/s step*1
25.600 004 to 32.100 000 Gbit/s / 0.000 004 Gbit/s step*2
–1000 to +1000 ppm / 1 ppm step*3

2.400 000 to 3.125 000 Gbit/s / 0.000 002 Gbit/s step
3.200 002 to 6.250 000 Gbit/s / 0.000 002 Gbit/s step
6.400 002 to 12.500 000 Gbit/s / 0.000 002 Gbit/s step
12.800 002 to 25.000 000 Gbit/s / 0.000 002 Gbit/s step
25.600 004 to 28.100 000 Gbit/s / 0.000 004 Gbit/s step*1
25.600 004 to 32.100 000 Gbit/s / 0.000 004 Gbit/s step*2
–1000 to +1000 ppm / 1 ppm step*3</td></tr>
<tr><td>External Clock
When the Output Clock Rate is set to Full Rate

When the Output Clock Rate is set to Half Rate</td><td>
<table>
<tr><th>Operating bit rate range</th><th>Input Clock Frequency</th><th>Relationship Between Bitrate and Clock Frequency</th></tr>
<tr><td>2.4 to 16.0 Gbit/s</td><td>2.4 to 16.0 Gbit/s</td><td>Operate at 1/1 clock</td></tr>
<tr><td>16.0 to 20.4 Gbit/s</td><td>8.0 to 10.2 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 to 28.1 Gbit/s*1</td><td>10.0 to 14.05 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 to 32.1 Gbit/s*2</td><td>10.0 to 16.05 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 28.1 Gbit/s*1</td><td>6.25 to 7.025 GHz</td><td>Operate at 1/4 clock</td></tr>
<tr><td>25.0 to 32.1 Gbit/s*2</td><td>6.25 to 8.025 Gbit/s</td><td>Operate at 1/4 clock</td></tr>
</table>
<table>
<tr><th>Operating bit rate range</th><th>Input Clock Frequency</th><th>Relationship Between Bitrate and Clock Frequency</th></tr>
<tr><td>2.4 to 28.1 Gbit/s*1</td><td>1.2 to 14.05 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>2.4 to 32.1 Gbit/s*2</td><td>1.2 to 16.05 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 28.1 Gbit/s*1</td><td>6.25 to 7.025 GHz</td><td>Operate at 1/4 clock</td></tr>
<tr><td>25.0 to 32.1 Gbit/s*2</td><td>6.25 to 8.025 Gbit/s</td><td>Operate at 1/4 clock</td></tr>
</table>
</td></tr>
</table>

Table 1.3.1-1 Operating Bit Rate (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Tracking with external clock
MU181500B
When the Output Clock Rate is set to Full Rate

When the Output Clock Rate is set to Half Rate</td><td>
<table>
<tr><th>Operating bit rate range</th><th>Input Clock Frequency</th><th>Relationship Between Bitrate and Clock Frequency</th></tr>
<tr><td>2.4 to 15.0 Gbit/s</td><td>2.4 to 15.0 Gbit/s</td><td>Operate at 1/1 clock</td></tr>
<tr><td>12.5 to 20.0 Gbit/s</td><td>6.25 to 10.0 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 to 28.1 Gbit/s*1</td><td>10.0 to 14.05 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 to 30.0 Gbit/s*2</td><td>10.0 to 16.05 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 32.1 Gbit/s*2</td><td>6.25 to 8.025 Gbit/s</td><td>Operate at 1/4 clock</td></tr>
</table>
<table>
<tr><th>Operating bit rate range</th><th>Input Clock Frequency</th><th>Relationship Between Bitrate and Clock Frequency</th></tr>
<tr><td>2.4 to 28.1 Gbit/s*1</td><td>1.2 to 14.05 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>2.4 to 30.0 Gbit/s*2</td><td>1.2 to 15.0 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>30.0 to 32.1 Gbit/s*2</td><td>7.5 to 8.025 Gbit/s</td><td>Operate at 1/4 clock</td></tr>
</table>
</td></tr>
</table>

Table 1.3.1-2 External Clock Input

Item	Specifications
Number of Input	1 (Single-Ended)
Input frequency range	1.2 to 16.05 GHz
Input amplitude	0.3 to 1.0 Vp-p (–6.5 to +4.0 dBm)
Termination	AC/50 Ω
Connector	SMA connector (f.)

Table 1.3.1-3 Aux Input and Output

Item	Specifications
Aux Input	
Number of Input	1 (Single-Ended)
Signal Type	Error Injection, Burst
Minimum Pulse Width	1/128 of data rate
Input level	0/–1 V (H: –0.25 to 0.05 V L: –1.1 to –0.8 V)
Termination	GND/50 Ω
Connector	SMA connector (f.)
Aux Output	
Number of Output	2 (Differential output)
Signal Type	1/n Clock (n=4, 6, 8, 10….510, 512), Pattern Sync, Burst Out2
Pattern Sync	
PRBS, PRGM	Position: 1 to {(Least common multiple of Pattern Length' and 128) –135}, in 8 steps When the pattern length is 511 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 512 bits or more.
Mixed Data	Block No. setting: 1 to the Block No. specified for Mixed Data, in single steps Row No. setting: 1 to the Row No. specified for Mixed Data, in single steps
Burst Out2	
Burst Trigger Delay	0 to (Burst Cycle – 128) bits / 8 bits step
Pulse Width	0 to (Burst Cycle – 128) bits / 8 bits step
Output level	0/–0.6 V (H: –0.25 to 0.05 V /L: –0.80 to –0.45 V)
Terminator	GND/50 Ω
Connector	SMA connector (f.)

Table 1.3.1-4 Gating output

Item	Specifications
Burst	Burst Output
Burst Trigger Delay	0 to (Burst Cycle – 128) bits / 8 bits step
Pulse Width	0 to (Burst Cycle – 128) bits / 8 bits step
Repeat	Timing Signal Output
Timing Signal Cycle	INT (Pattern Length / 128) × 128 (other than Mixed)
Timing Signal Pulse Width	For PRBS, Zero-Substitution, Data: 0 to {(Least common multiple of Pattern Length' and 128) –128}, in 8-bit steps The maximum settable number is 34 359 738 240. When the pattern length is 511 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 512 bits or more. For Mixed: 0 to (Row length × Number of rows × Number of blocks –128), in 8-bit steps The maximum settable number is 2 415 918 976.
Timing Signal Delay	Same value as the timing signal pulse width.
Output level	0/–1 V (H: –0.25 to 0.05 V, L: –1.25 to –0.8 V)
Terminator	GND/50 Ω
Connector	SMA connector (f.)

Table 1.3.1-5 Generated pattern

Item	Specifications
PRBS	
Pattern Length	2^n-1 (n = 7, 9, 10, 11, 15, 20, 23, 31)
Mark ratio	1/2 (1/2INV is supported by a logical inversion.)
Zero-Substitution	
Additional bit	0 bit, 1 bit
Pattern Length	2^n (n = 7, 9, 10, 11, 15, 20, 23) 2^n-1 (n = 7, 9, 10, 11, 15, 20, 23)
Start position	Substitutes the bit coming after the maximum "0" successive bits.
Length of Consecutive Zero Bits	1 to (Pattern Length–1) bits If the bit coming after Zero-substitution is "0", then it is replaced with "1".
Data	
Data Length	2 to 268 435 456 bits / 1 bit step
Mixed Pattern	
Pattern	Data
Mixed Block	To the smaller of the following values: 1 to 511 Block / 1 Block step $\mathrm{INT}\left(\frac{268435456}{\text{ROW count}} \times \text{Data length}\right)$ bits $\mathrm{INT}\left(\frac{2415919104}{\text{ROW length}} \times \text{ROW count}\right)$ bits
Mixed Row Length	1 536 to 2 415 919 104 / 256 bits step (Data + PRBS Length)
Data Length	1 024 to 268 435 456 bits / 1 bit step
Number of rows	1 to 16 / 1 step
Number of blocks	1 to 511 / 1 step
PRBS Pattern Length / Mark ratio	Same as PRBS.
PRBS Sequence	Restart, Consecutive
Scramble	Can be set per PRBS and Data for each Block (except the Data area for Block 1)

Table 1.3.1-6 Pattern Sequence

Item	Specifications
Sequence	Repeat/Burst
Repeat	Continuous Pattern
Burst	
Source	Internal, External-Trigger (Aux Input), External-Enable (Aux Input)
Data Sequence	Restart, Consecutive, Continuous
Burst Cycle	25 600 to 2 147 483 648 bits / 256 bits step
Enable period	Internal: 12 800 to 2 147 483 392 bits / 256 bits step
	Ext Trigger, Enable: 12 800 to 2 147 483 648 bits / 256 bits step

Table 1.3.1-7 Pre-Code

Item	Specifications
ON/OFF	Sets Pre-Code function ON and OFF
Type	Sets Pre-Code modulation method
	2ch Combination: DQPSK
Initial Data	Sets Pre-Code defaults
	Choose 0 or 1.

Table 1.3.1-8 Error addition

Item	Specifications
Area	ALL, Specific Block (Can be selected only for Mixed.)
Internal trigger	
Error Variation	Repeat, Single
Error Ratio	$A \times 10^{-b}$ (a=1 to 9, b=3 to 12)*
Insertion CH	1 to 32, or channel scan (Only when Internal is set.)
External trigger	
Control Method	External-Trigger (Rise edge trigger), External-Disable (L: Disable)

*: Upper limit is 5E–3.

Table 1.3.1-9 Data Output

Item	Specifications*1
Number of outputs	Option x12/x13:2 (Data, XData (Independent)) Option x22/x23:4 (Data1, XData1, Data2, XData2 (Independent))
Output amplitude	
Setting range	Option x12/x22: 0.5 to 2.0 Vp-p / 2 mV step Option x13/x23: 0.5 to 3.5 Vp-p / 2 mV step
Setting error	±50 mV± (17% of set Amplitude)*2
Offset	
Reference level	Voh, Vth, Vol
Setting range	Voh: –2.0 to +3.3 V / 1 mV step Minimum value Vol: –4.0 V
Setting error	±65 mV ±10% of offset (Vth) ± (Output amplitude setting error/ 2)
Current limitation	Sourcing 50 mA Sinking 80 mA
Defined Interface	NECL, SCFL, NCML, PCML, LVPECL
Cross Point	
Setting range	20 to 80% / 0.1% step (Amplitude: 1.0 to 2.0 Vp-p for option x12/x22) (Amplitude: 1.0 to 3.5 Vp-p for option x13/x23) 30 to 70% / 0.1% step (Amplitude: 0.5 to 0.998 Vp-p)
Rising/falling time	12 ps (20 to 80%)*3,*4,*5
Half Period Jitter	–20 to 20 / 1 step

*1: Unless otherwise specified, these are defined with the conditions of PRBS2^{31}–1, Mark ratio 1/2, and Cross Point 50%.

These values are monitored using an applicable part (J1439A coaxial cable, 0.8 m, K connector) at a sampling oscilloscope bandwidth of 70 GHz.

*2: Under the following conditions:

Option x01	Bit Rate	Cross Point
Not available	25 Gbit/s and 28.1 Gbit/s	30 to 80%
	Full range except 25 Gbit/s and 28.1 Gbit/s	50%
Available	25 Gbit/s and 32.1 Gbit/s	30 to 80%
	Full range except 25 Gbit/s and 32.1 Gbit/s	50%

*3: If Option x01 is not available, then this is at 28.1 Gbit/s.

If Option x01 is available, then this is at 32.1 Gbit/s.

*4: Amplitude: 2.0 Vp-p for option x12/x22

Amplitude: 3.5 Vp-p for option x13/x23

*5: Typical value

Table 1.3.1-9 Data Output (Cont'd)

Item	Specifications*1
Jitter	Jitter (p-p): 8 ps p-p*3,*4,*5,*6 Jitter (RMS): 700 fs*3,*4, *5,*6 Intrinsic RJ (RMS): 300 fs*3,*4,*5,*6,*8
Waveform Distortion (0-peak)	±25 mV ±15%*3,*4,*5
Output control	ON/OFF switching
Skew between channels*7	±0.25 UI*9
Termination	AC/DC switching, 50 Ω For DC: GND, –2 V, +1.3 V, +3.3 V, Open
Connector	K (f.)
Data/XData Tracking	This can be performed by operation on the screen.
Level Guard	Amplitude, Voh, and Vol can be specified.
External ATT factor	0 to 40 dB / 1 dB step

*6: Using oscilloscope with residual jitter of less than 200 fs (RMS).

*7: When Option x22 or Option x23 is available.

*8: Defined with a repetition pattern of "1" and "0"

*9: When Option x31 is available.

Table 1.3.1-10 Clock Output

Item	Specifications*1
Frequency	
Full Rate	2.4 to 28.1 GHz*2 2.4 to 32.1 GHz*3 Operation bit rate is same as clock output frequency.
Half Rate	1.2 to 14.05 GHz*2 1.2 to 16.05 GHz*3 Operation bit rate is half of clock output frequency.
Number of Output	1
Amplitude	0.3 to 1.0 Vp-p
Output control	ON/OFF switching
Termination	AC/50 Ω
Connector	K (f.)

*1: These values are monitored using an applicable part (J1439A coaxial cable, 0.8 m, K connector) at a sampling oscilloscope bandwidth of 70 GHz.

*2: Option x01 not available.

*3: Option x01 available.

Table 1.3.1-11 Data Delay*1

Item	Specifications
Phase variable range	–1 000 to +1 000 mUI / 2 mUI step
Phase setting error	±50 mUIp-p*2,*3,*4 ±75 mUIp-p*2,*3,*5
mUI – ps switching	Available
Calibration	Available
Calibration indicator	This indicator is on when Calibration is required due to: • 1/1 Clock frequency change by ±250 kHz. • Ambient temperature change by ±5 degree.

*1: When Option x30 or Option x31 is available.

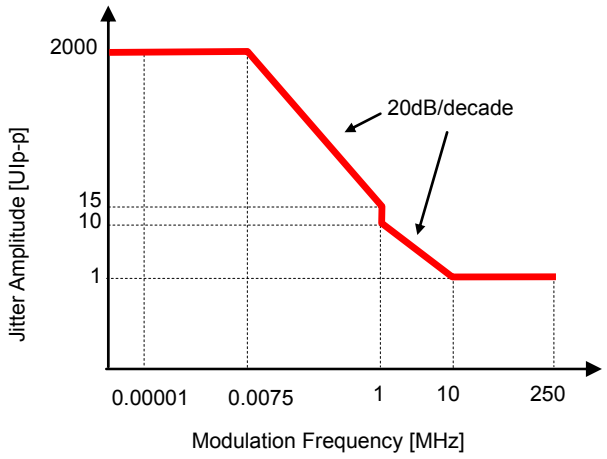
*2: When using an item with an oscilloscope residual jitter of less than 200 fs (RMS).

*3: Typical value

*4: Bit rate ≤ 28.1 Gbit/s

*5: Bit rate > 28.1 Gbit/s

Table 1.3.1-12 Jitter tolerance

Item	Specifications
Jitter tolerance mask*3	Bit rate: 16 Gbit/s, 28.1 Gbit/s*1 16 Gbit/s, 28.1 Gbit/s, 32.1 Gbit/s*2 Pattern: PRBS $2^{31}-1$ Temperature: 20 to 30°C SSC with a 5300 ppm amplitude and RJ of 0.3 UI can be simultaneously applied by using MU181500B. These specifications are defined assuming the following conditions: ・Loopback connection with MU183040A/41A. 

*1: Option x01 not available.

*2: Option x01 available.

*3: The tolerance will be extended in Version 7.09.00 or any later version of MX180000A.

Table 1.3.1-13 Multichannel operation

Item	Specifications
Combination Setting*1, *2	
2ch Combination	Alternately outputs each bit in pattern as 56/64 Gbit/s band signal source to two channels.
Channel Synchronization*1	
Number of channels	2 to 4*3
Output	
Phase variable range	–64 000 to +64 000 mUI*4
Phase variable step	2 mUI *4
Pattern	
Data	
Data Length	4 to 536 870 912 bits / 2 bits step*5
Mixed	
Row Length	3 072 to 4 831 838 208 / 512 bits step*5
Data Length	2 048 to 536 870 912 bits / 2 bits step*5
Burst	
Burst Cycle	51 200 to 4 294 967 296 bits / 512 bits step*5
Enable period	Internal: 25 600 to 4 294 966 784 bits / 512 bits step*5 Ext Trigger, Enable: 25 600 to 4 294 967 296 bits / 512 bits step*5
Delay	0 to (Burst Cycle – 128) × 2 bits / 16 bits step*5
Pulse Width	0 to (Burst Cycle – 128) × 2 bits / 16 bits step*5
Gating Output Repeat (Data)	
Pulse Width	0 to 68 719 476 480 / 16 bits step*5
Delay	0 to 68 719 476 480 / 16 bits step*5
Repeat (Mixed)	
Pulse Width	0 to 4 831 837 952 / 16 bits step*5
Delay	0 to 4 831 837 952 / 16 bits step*5

*1: Option x31 is required for target channels.

*2: Combination extending over multiple slots cannot be set.

*3: When target channels are installed successively from Slot 1.

*4: A separate value can be set for each channel. This value is common to both Channel Combination and Channel Synchronization.

*5: Common to every channel specified by Combination Setting.

Table 1.3.1-14 General

Item	Specifications
Dimensions	21 mm (H), 234 mm (W), 175 mm (D) Excluding protrusions
Mass	2.5 kg max.
Operating Temperature	15 to 35°C
Storage Temperature	–20 to 60°C

1.3.2 Specifications for MU183021A

Table 1.3.2-1 Operating Bit Rate

Item	Specifications
MU181000A/B synchronized operation ON	This item can be specified when MU181000A or MU181000B are installed to the same unit.
When the Output Clock Rate is set to Full Rate	
Setting Range	2.400 000 to 12.500 000 Gbit/s / 0.000 001 Gbit/s step 12.500 002 to 20.000 000 Gbit/s / 0.000 002 Gbit/s step 20.000 002 to 25.000 000 Gbit/s / 0.000 002 Gbit/s step 25.000 004 to 28.100 000 Gbit/s / 0.000 004 Gbit/s step*1 25.000 004 to 32.100 000 Gbit/s / 0.000 004 Gbit/s step*2
Offset	–1000 to +1000 ppm / 1 ppm step*3
When the Output Clock Rate is set to Half Rate	
Setting Range	2.400 000 to 25.000 000 Gbit/s / 0.000 002 Gbit/s step 25.000 004 to 28.100 000 Gbit/s / 0.000 004 Gbit/s step*1 25.000 004 to 32.100 000 Gbit/s / 0.000 004 Gbit/s step*2
Offset	–1000 to +1000 ppm / 1 ppm step*3

*1: Not available Option x01

*2: Available Option x01

*3: The setting range varies depending on the bit rate setting. At following bit rate setting, setting range is from –1000 to 0 ppm.

Full rate: 12.500000 Gbit/s, 25.000000 Gbit/s

Half rate: 25.000000 Gbit/s

Table 1.3.2-1 Operating Bit Rate (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>MU181500B synchronized operation ON
When the Output Clock Rate is set to Full Rate
Setting Range

Offset
When the Output Clock Rate is set to Half Rate
Setting Range

Offset</td><td>This item can be specified when MU181000A, MU181000B and MU181500B are installed to the same unit.

2.400 000 to 3.125 000 Gbit/s / 0.000 001 Gbit/s step
3.200 001 to 6.250 000 Gbit/s / 0.000 001 Gbit/s step
6.400 001 to 12.500 000 Gbit/s / 0.000 001 Gbit/s step
12.800 002 to 15.000 000 Gbit/s / 0.000 002 Gbit/s step
15.000 002 to 20.000 000 Gbit/s / 0.000 002 Gbit/s step
20.000 002 to 25.000 000 Gbit/s / 0.000 002 Gbit/s step
25.600 004 to 28.100 000 Gbit/s / 0.000 004 Gbit/s step*1
25.600 004 to 32.100 000 Gbit/s / 0.000 004 Gbit/s step*2
–1000 to +1000 ppm / 1 ppm step*3

2.400 000 to 3.125 000 Gbit/s / 0.000 002 Gbit/s step
3.200 002 to 6.250 000 Gbit/s / 0.000 002 Gbit/s step
6.400 002 to 12.500 000 Gbit/s / 0.000 002 Gbit/s step
12.800 002 to 25.000 000 Gbit/s / 0.000 002 Gbit/s step
25.600 004 to 28.100 000 Gbit/s / 0.000 004 Gbit/s step*1
25.600 004 to 32.100 000 Gbit/s / 0.000 004 Gbit/s step*2
–1000 to +1000 ppm / 1 ppm step*3</td></tr>
<tr><td>External Clock
When the Output Clock Rate is set to Full Rate

When the Output Clock Rate is set to Half Rate</td><td>
<table>
<tr><th>Operating bit rate range</th><th>Input Clock Frequency</th><th>Relationship Between Bitrate and Clock Frequency</th></tr>
<tr><td>2.4 to 16.0 Gbit/s</td><td>2.4 to 16.0 Gbit/s</td><td>Operate at 1/1 clock</td></tr>
<tr><td>16.0 to 20.4 Gbit/s</td><td>8.0 to 10.2 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 to 28.1 Gbit/s*1</td><td>10.0 to 14.05 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 to 32.1 Gbit/s*2</td><td>10.0 to 16.05 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 28.1 Gbit/s*1</td><td>6.25 to 7.025 GHz</td><td>Operate at 1/4 clock</td></tr>
<tr><td>25.0 to 32.1 Gbit/s*2</td><td>6.25 to 8.025 Gbit/s</td><td>Operate at 1/4 clock</td></tr>
</table>
<table>
<tr><th>Operating bit rate range</th><th>Input Clock Frequency</th><th>Relationship Between Bitrate and Clock Frequency</th></tr>
<tr><td>2.4 to 28.1 Gbit/s*1</td><td>1.2 to 14.05 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>2.4 to 32.1 Gbit/s*2</td><td>1.2 to 16.05 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 28.1 Gbit/s*1</td><td>6.25 to 7.025 GHz</td><td>Operate at 1/4 clock</td></tr>
<tr><td>25.0 to 32.1 Gbit/s*2</td><td>6.25 to 8.025 Gbit/s</td><td>Operate at 1/4 clock</td></tr>
</table>
</td></tr>
</table>

Table 1.3.2-1 Operating Bit Rate (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Tracking with external clock
MU181500B
When the Output Clock Rate is set to Full Rate

When the Output Clock Rate is set to Half Rate</td><td>
<table>
<tr><th>Operating bit rate range</th><th>Input Clock Frequency</th><th>Relationship Between Bitrate and Clock Frequency</th></tr>
<tr><td>2.4 to 15.0 Gbit/s</td><td>2.4 to 15.0 Gbit/s</td><td>Operate at 1/1 clock</td></tr>
<tr><td>12.50 to 20.0 Gbit/s</td><td>6.25 to 10.0 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 to 28.1 Gbit/s*1</td><td>10.0 to 14.05 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 to 30.0 Gbit/s*2</td><td>10.0 to 16.05 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 32.1 Gbit/s*2</td><td>6.25 to 8.025 Gbit/s</td><td>Operate at 1/4 clock</td></tr>
</table>
<table>
<tr><th>Operating bit rate range</th><th>Input Clock Frequency</th><th>Relationship Between Bitrate and Clock Frequency</th></tr>
<tr><td>2.4 to 28.1 Gbit/s*1</td><td>1.2 to 14.05 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>2.4 to 30.0 Gbit/s*2</td><td>1.2 to 15.0 Gbit/s</td><td>Operate at 1/2 clock</td></tr>
<tr><td>30.0 to 32.1 Gbit/s*2</td><td>7.5 to 8.025 Gbit/s</td><td>Operate at 1/4 clock</td></tr>
</table>
</td></tr>
</table>

Table 1.3.2-2 External Clock Input

Item	Specifications
Number of Input	1 (Single-Ended)
Input frequency range	1.2 to 16.05 GHz
Input amplitude	0.3 to 1.0 Vp-p (–6.5 to +4.0 dBm)
Termination	AC/50 Ω
Connector	SMA connector (f.)

Table 1.3.2-3 Aux Input and Output

Item	Specifications
Aux Input	
Number of Input	1 (Single-Ended)
Signal Type	Error Injection, Burst
Minimum Pulse Width	1/128 of data rate
Input level	0/–1 V (H: –0.25 to 0.05 V, L: –1.1 to –0.8 V)
Termination	GND/50 Ω
Connector	SMA connector (f.)
Aux Output	
Number of Output	2 (Differential output)
Signal Type	1/n Clock (n=4, 6, 8, 10…..510, 512), Pattern Sync, Burst Out2
Pattern Sync	
PRBS, PRGM	Position: 1 to {(Least common multiple of Pattern Length' and 128) – 135}, in 8 steps When the pattern length is 511 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 512 bits or more.
Mixed Data	Block No. setting: 1 to the Block No. specified for Mixed Data, in single steps Row No. setting: 1 to the Row No. specified for Mixed Data, in single steps
Burst Out2	
Burst Trigger Delay	0 to (Burst Cycle – 128) bits / 8 bits step
Pulse Width	0 to (Burst Cycle – 128) bits / 8 bits step
Output level	0/–0.6 V (H: –0.25 to 0.05 V /L: –0.80 to –0.45 V)
Terminator	GND/50 Ω
Connector	SMA connector (f.)

Table 1.3.2-4 Gating output

Item	Specifications
Burst	Burst Output
Burst Trigger Delay	0 to (Burst Cycle – 128) bits / 8 bits step
Pulse Width	0 to (Burst Cycle – 128) bits / 8 bits step
Repeat	Timing Signal Output
Timing Signal Cycle	INT (Pattern Length / 128) × 128 (other than Mixed)
Timing Signal Pulse Width	For PRBS, Zero-Substitution, Data: 0 to {(Least common multiple of Pattern Length' and 128) –128},in 8-bit steps The maximum settable number is 34 359 738 240. When the pattern length is 511 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 512 bits or more. For Mixed: 0 to (Row length × Number of rows × Number of blocks –128), in 8-bit steps The maximum settable number is 2 415 918 976.
Timing Signal Delay	Same value as the timing signal pulse width.
Output level	0/–1 V (H: –0.25 to 0.05 V, L: –1.25 to –0.8 V)
Terminator	GND/50 Ω
Connector	SMA connector (f.)

Table 1.3.2-5 Generated pattern

Item	Specifications
PRBS	
Pattern Length	2^n-1 (n = 7, 9, 10, 11, 15, 20, 23, 31)
Mark ratio	1/2 (1/2INV is supported by a logical inversion.)
Zero-Substitution	
Additional bit	0 bit, 1 bit
Pattern Length	2^n (n = 7, 9, 10, 11, 15, 20, 23) 2^n-1 (n = 7, 9, 10, 11, 15, 20, 23)
Start position	Substitutes the bit coming after the maximum "0" successive bits.
Length of Consecutive Zero Bits	1 to (Pattern Length–1) bits If the bit coming after Zero-substitution is "0", then it is replaced with "1".
Data	
Data Length	2 to 268 435 456 bits / 1 bit step
Mixed Pattern	
Pattern	Data
Mixed Block	To the smaller of the following values: 1 to 511 Block / 1 Block step $\mathrm{INT}\left(\frac{268435456}{\text{ROW count}} \times \text{Data length}\right)$ bits $\mathrm{INT}\left(\frac{2415919104}{\text{ROW length}} \times \text{ROW count}\right)$ bits
Mixed Row Length	1 536 to 2 415 919 104 / 256 bits step (Data + PRBS Length)
Data Length	1 024 to 268 435 456 bits / 1 bit step
Number of rows	1 to 16 / 1 step
Number of blocks	1 to 511 / 1 step
PRBS Pattern Length / Mark ratio	Same as PRBS.
PRBS Sequence	Restart, Consecutive
Scramble	Can be set per PRBS and Data for each Block (except the Data area for Block 1)

Table 1.3.2-6 Pattern Sequence

Item	Specifications
Sequence	Repeat/Burst
Repeat	Continuous Pattern
Burst	
Source	Internal, External-Trigger (AUX Input), External-Enable (AUX Input)
Data Sequence	Restart, Consecutive, Continuous
Burst Cycle	25 600 to 2 147 483 648 bits / 256 bits step
Enable period	Internal: 12 800 to 2 147 483 392 bits / 256 bits step
	Ext Trigger, Enable: 12 800 to 2 147 483 648 bits / 256 bits step

Table 1.3.2-7 Pre-Code

Item	Specifications
ON/OFF	Sets Pre-Code function ON and OFF
Type	Sets Pre-Code modulation method
	2ch Combination: DQPSK
	2ch CH Sync: DPQPSK
Initial Data	Sets Pre-Code defaults
	Choose 0 or 1.

Table 1.3.2-8 Error addition

Item	Specifications
Area	ALL, Specific Block (Can be selected only for Mixed.)
Internal trigger	
Error Variation	Repeat, Single
Error Ratio	$a \times 10^{-b}$ (a=1 to 9, b=3 to 12)*
Insertion CH	1 to 32, or channel scan (Only when Internal is set.)
External trigger	
Control Method	External-Trigger (Rise edge trigger), External-Disable (L: Disable)

*: Upper limit is 5E–3.

Table 1.3.2-9 Data Output

Item	Specifications*1
Number of outputs	8 (Data1, XData1 to Data4, XData4 (Independent))
Output amplitude	
Setting range	Option x12: 0.5 to 2.0 Vp-p / 2 mV step Option x13: 0.5 to 3.5 Vp-p / 2 mV step
Setting error	±50 mV ±(17% of set Amplitude)*2
Offset	
Reference level	Voh, Vth, Vol
Setting range	Voh: –2.0 to +3.3 V / 1 mV step Minimum value Vol: –4.0 V
Setting error	±65 mV ±10% of offset(Vth)±(Output amplitude setting error/ 2)
Current limitation	Sourcing 50 mA Sinking 80 mA
Defined Interface	NECL, SCFL, NCML, PCML, LVPECL
Cross Point	
Setting range	20 to 80% / 0.1% step (Amplitude: 1.0 to 2.0 Vp-p for option x12) (Amplitude: 1.0 to 3.5 Vp-p for option x13) 30 to 70% / 0.1% step (Amplitude: 0.5 to 0.998 Vp-p)
Rising/falling time	12 ps (20 to 80%)*3,*4,*5
Half Period Jitter	–20 to 20 / 1 step

*1: Unless otherwise specified, these are defined with the conditions of PRBS2^{31}–1, Mark ratio 1/2, and Cross Point 50%.

These values are monitored using an applicable part (J1439A coaxial cable, 0.8 m, K connector) at a sampling oscilloscope bandwidth of 70 GHz.

*2: Under the following conditions:

Option x01	Bit Rate	Cross Point
Not available	25 Gbit/s and 28.1 Gbit/s	30 to 80%
	Full range except 25 Gbit/s and 28.1 Gbit/s	50%
Available	25 Gbit/s and 32.1 Gbit/s	30 to 80%
	Full range except 25 Gbit/s and 32.1 Gbit/s	50%

*3: If option x01 is not available, then this is at 28.1 Gbit/s.

If option x01 is available, then this is at 32.1 Gbit/s.

*4: Amplitude: 2.0 Vp-p for option x12

Amplitude: 3.5 Vp-p for option x13

*5: Typical value

Table 1.3.2-9 Data Output (Cont'd)

Item	Specifications*1
Jitter	Jitter (p-p): 8 ps p-p*3,*4,*5,*6 Jitter (RMS): 700 fs*3,*4,*5,*6 Intrinsic RJ (RMS): 300 fs*3,*4, *5,*6,*7
Waveform Distortion (0-peak)	±25 mV ±15%*3,*4,*5
Output control	ON/OFF switching
Skew between channels	±0.25 UI*8
Termination	AC/DC switching, 50 Ω For DC: GND, –2 V, +1.3 V, +3.3 V, Open
Connector	K (f.)
Data/XData Tracking	This can be performed by operation on the screen.
Level Guard	Amplitude, Voh, and Vol can be specified.
External ATT Factor	0 to 40 dB / 1 dB step

*6: Using oscilloscope with residual jitter of less than 200 fs (RMS).

*7: Defined with a repetition pattern of "1" and "0"

*8: If Option x30 is available.

Table 1.3.2-10 Clock Output

Item	Specifications*1
Frequency	
Full Rate	2.4 to 28.1 GHz*2 2.4 to 32.1 GHz*3 Operation bit rate is same as clock output frequency.
Half Rate	1.2 to 14.05 GHz*2 1.2 to 16.05 GHz*3 Operation bit rate is half of clock output frequency.
Number of Output	1
Amplitude	0.3 to 1.0 Vp-p
Output control	ON/OFF switching
Termination	AC/50 Ω
Connector	K (f.)

*1: These values are monitored using an applicable part (J1439A coaxial cable, 0.8 m, K connector) at a sampling oscilloscope bandwidth of 70 GHz.

*2: Option x01 not available.

*3: Option x01 available.

Table 1.3.2-11 Data Delay*1

Item	Specifications
Phase variable range	–1 000 to +1 000 mUI / 2 mUI step
Phase setting error	±50 mUIp-p*2,*3,*4 ±75 mUIp-p*2,*3,*5
mUI – ps switching	Available
Calibration	Available
Calibration indicator	This indicator is on when Calibration is required due to: ・Change in 1/1Clock frequency by ±250 kHz. ・Change in the ambient temperature by ±5°C.

*1: When MU183021A-x30 is installed.

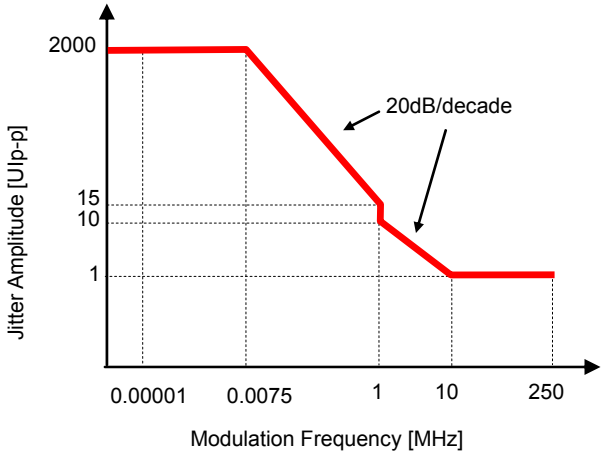
*2: When using an item with an oscilloscope residual jitter of less than 200 fs (RMS).

*3: Typical value

*4: Bit rate ≤ 28.1 Gbit/s

*5: Bit rate > 28.1 Gbit/s

Table 1.3.2-12 Jitter tolerance

Item	Specifications
Jitter tolerance mask*3	Bit rate: 16 Gbit/s, 28.1 Gbit/s*1 16 Gbit/s, 28.1 Gbit/s, 32.1 Gbit/s*2 Pattern: PRBS $2^{31}-1$ Temperature: 20 to 30°C SSC with a 5300 ppm amplitude and RJ of 0.3 UI can be simultaneously applied by using MU181500B. These specifications are defined assuming the following conditions: ・Loopback connection with MU183040A/41A. 

*1: Option x01 not available.

*2: Option x01 available.

*3: The tolerance will be extended in Version 7.09.00 or any later version of MX180000A.

Table 1.3.2-13 Multichannel operation

Item	Specifications
Combination Setting*1,*2	
2ch/4ch Combination	· Alternately outputs each bit in pattern as 56/64 Gbit/s band signal source to two channels. Or · Alternately outputs each bit in pattern as 112/128 Gbit/s band signal source to four channels.
2ch CH Sync	Synchronizes two 56/64 Gbit/s Combination signals and outputs them.
Channel Synchronization*1	
Number of channels	2 to 8*3
Output	
Phase variable range	–64 000 to +64 000 mUI*4
Phase variable step	2 mUI *4
Pattern	
Data	
Data Length	4 to 536 870 912 bits / 2 bits step*5 8 to 1 073 741 824 bits / 4 bits step*6
Mixed	
Row Length	3 072 to 4 831 838 208 / 512 bits step*5 6 144 to 9 663 676 416 / 1024 bits step*6
Data Length	2 048 to 536 870 912 bits / 2 bits step*5 4 096 to 1 073 741 824 bits / 4 bits step*6
Burst	
Burst Cycle	51 200 to 4 294 967 296 bits / 512 bits step*5 102 400 to 8 589 934 592 bits / 1024 bits step*6
Enable period	Internal: 25 600 to 4 294 966 784 bits / 512 bits step*5 51 200 to 8 589 933 568 bits / 1024 bits step*6 Ext Trigger, Enable: 25 600 to 4 294 967 296 bits / 512 bits step*5 51 200 to 8 589 934 592 bits / 1024 bits step*6
Delay	0 to (Burst Cycle–128) × 2 bits / 16 bits step*5 0 to (Burst Cycle–128) × 4 bits / 32 bits step*6
Pulse Width	0 to (Burst Cycle–128) × 2 bits / 16 bits step*5 0 to (Burst Cycle–128) × 4 bits / 32 bits step*6

*1: Option x30 is required for target channels.

*2: Combination extending over multiple slots cannot be set.

*3: When target channels are installed successively from Slot 1.

*4: A separate value can be set for each channel. This value is common to both Channel Combination and Channel Synchronization.

*5: Common to all the channels specified as 2ch Combination.

*6: Common to all the channels specified as 4ch Combination.

Table 1.3.2-13 Multichannel operation (Cont'd)

Item	Specifications
Gating Output Repeat (Data)	
Pulse Width	0 to 68 719 476 480 / 16 bits step*5
	0 to 137 438 952 960 / 32 bits step*6
Delay	0 to 68 719 476 480 / 16 bits step*5
	0 to 137 438 952 960 / 32 bits step*6
Repeat (Mixed)	
Pulse Width	0 to 4 831 837 952 / 16 bits step*5
	0 to 9 663 675 904 / 32 bits step*6
Delay	0 to 4 831 837 952 / 16 bits step*5
	0 to 9 663 675 904 / 32 bits step*6

Table 1.3.2-14 General

Item	Specifications
Dimensions	41 mm (H), 234 mm (W), 175 mm (D) Excluding protrusions
Mass	5 kg max.
Operating Temperature	15 to 35°C
Storage Temperature	–20 to 60°C

Chapter 2 Before Use

This chapter describes preparations required before using the MU183020A/MU183021A.

2.1 Installation to Signal Quality Analyzer

For information on how to install the MU183020A/MU183021A to the Signal Quality Analyzer and how to turn on the power, refer to Chapter 2 “Preparation before Use” in the Signal Quality Analyzer Series Installation Guide.

2.2 How to Operate Application

The modules connected to the Signal Quality Analyzer are controlled by operating the MX180000A Signal Quality Analyzer Control Software (hereinafter, referred to as “MX180000A”).

For information on how to start up, shut down, and operate the MX180000A, refer to the *MX180000A Signal Quality Analyzer Control Software Operation Manual.*

2.3 Preventing Damage

Always observe the ratings when connecting to the input and output connectors of the MU183020A/MU183021A. If an out-of-range signal is input, the MU183020A/MU183021A may be damaged.

⚠ CAUTION

- **When signals are input to the MU183020A/MU183021A, avoid excessive voltage beyond the rating. Otherwise, the circuit may be damaged.**
- **When output is used at the 50 Ω GND terminator, never feed any current or input signals to the output.**
- **As a countermeasure against static electricity, ground other devices to be connected (including experimental circuits) with ground wires before connecting the I/O connector.**
- **The outer conductor and core of the coaxial cable may become charged as a capacitor. Use any metal to discharge the outer conductor and core before use.**
- **Never open the MU183020A/MU183021A. If you open it and MU183020A/MU183021A has failed or sufficient performance cannot be obtained, we may decline to repair the MU183020A/MU183021A.**
- **The MU183020A/MU183021A has many important circuits and parts including hybrid ICs. These parts are extremely sensitive to static electric charges, so never open the case of the MU183020A/MU183021A.**
- **The hybrid ICs used in the MU183020A/MU183021A are sealed in airtight containers; never open them. If you open it and the MU183020A/MU183021A has failed or sufficient performance cannot be obtained, we may decline to repair the MU183020A/MU183021A.**

⚠ CAUTION

- **To protect the MU183020A/MU183021A from electrostatic discharge failure, a conductive sheet should be placed onto the workbench, and the operator should wear an electrostatic discharge wrist strap. Always ground the wrist strap to the workbench antistatic mat or the frame ground of the MU183020A/MU183021A.**

- **When connecting an external device such as a Bias-T to the output connectors of this equipment, if the output signal includes any DC voltage, variations in the output of the DC power supply or load may change the level of the output signal, risking damage to the internal circuits.**

  - **Do not connect or disconnect any external devices while DC voltage is impressed.**

  - **Only switch DC power sources ON and OFF when all equipment connections have been completed.**

<Recommended procedure>

Measurement Preparation 1:

1. **Connect all equipment.**
2. **Set the DC power supply output to ON.**
3. **Set the equipment output to ON and complete measurement.**

Measurement Preparation 2

1. **Set the equipment output to OFF.**
2. **Set the DC power supply output to OFF.**
3. **Disconnect the equipment, or change the DUT connections.**

- **Since even unforeseen fluctuations in DC voltage and load (open or short circuits at the equipment output side and changes caused by using a high-frequency probe, etc.,) can damage the DUT and equipment, we recommend connecting a 50–ohm resistance in series with the DC terminal of the Bias-T to prevent risk of damage.**

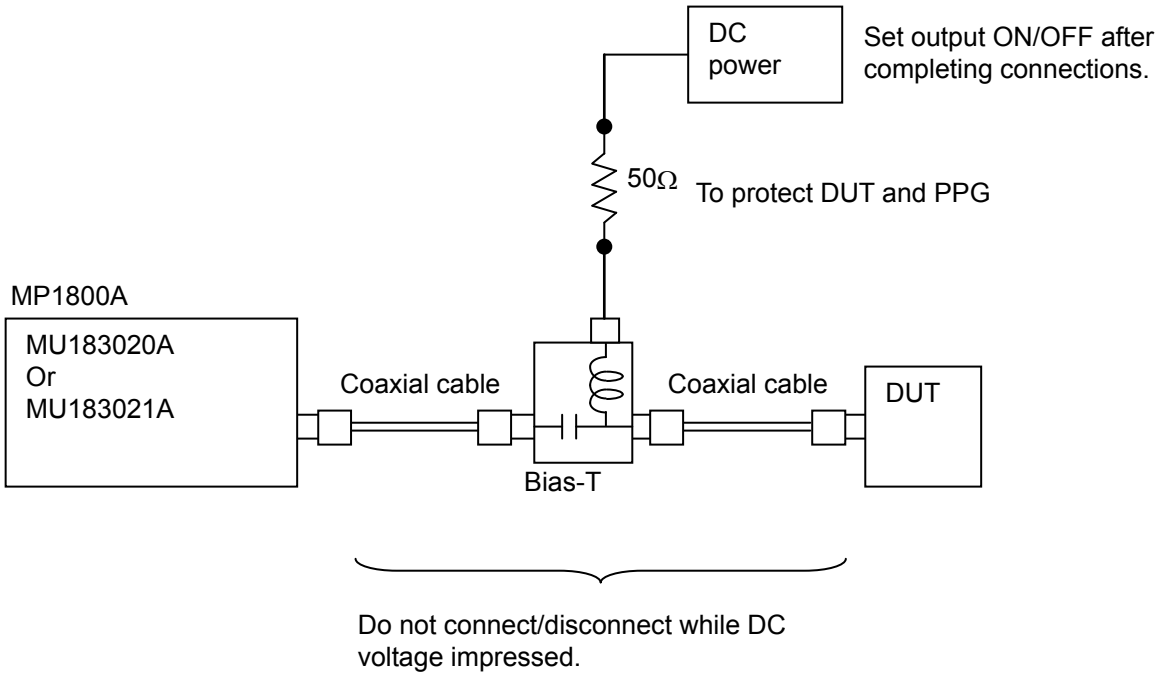


Figure 2.3-1 Bias-T Connection Example

Chapter 3 Panel Layout and Connectors

This chapter describes the panel and connectors of the MU183020A/MU183021A.

3.1 Panel Layout

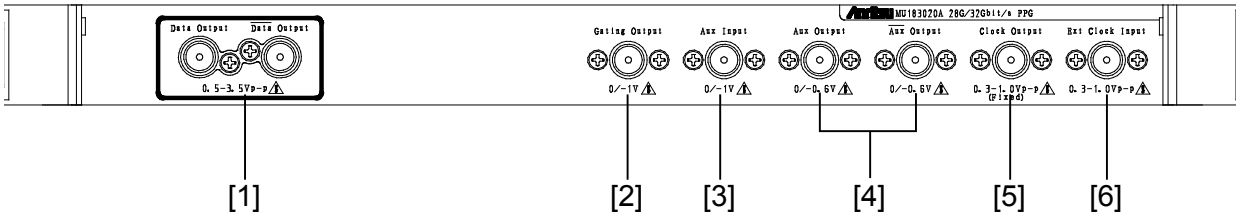


Figure 3.1-1 Panel layout (MU183020A-x12/x13)

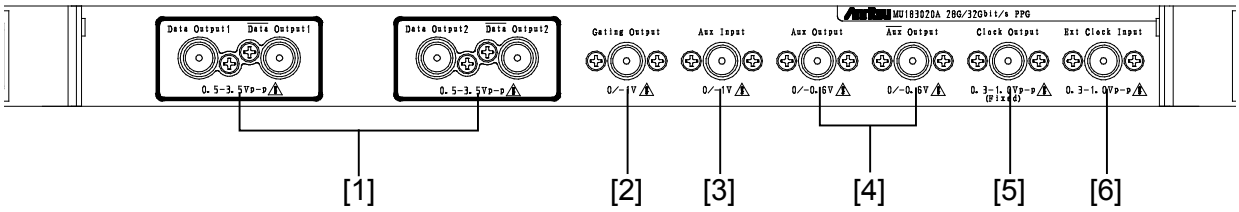


Figure 3.1-2 Panel layout (MU183020A-x22/x23)

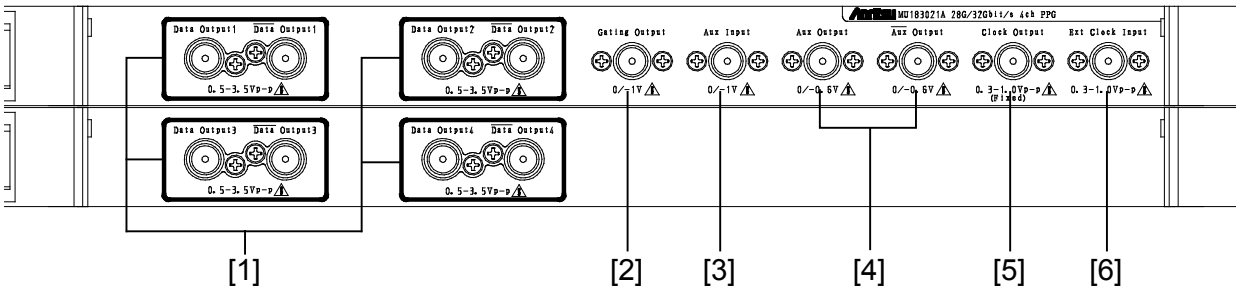


Figure 3.1-3 Panel layout (MU183021A)

Table 3.1-1 Connectors on MU183020A/MU183021A panel

No.	Name	Description
[1]	Data and $\overline{\text{Data}}$ Output connectors	Outputs the differential data signals . Various interface signals can be output, depending on the installed option (s).
[2]	Gating Output connector	In case of Repeat:Outputs the timing signals. In case of Burst: Outputs the timing signals for Burst.
[3]	Aux Input connector	Inputs auxiliary signals. Error Injection, and Burst can be selected.
[4]	Aux, $\overline{\text{Aux}}$ Output connector	Outputs auxiliary signals. 1/N clock, Pattern Sync, and Burst2 can be output according to the setting. Because of differential output, be sure to terminate the unused connector with the coaxial terminator (J1137).
[5]	Clock Output connectors	Outputs clock signals.
[6]	Ext Clock Input Connector	Inputs clock signals from these units: MU181000A 12.5GHz Synthesizer MU181000B 12.5GHz 4 Ports Synthesizer MU181500B Jitter Modulation Source*1 External Synthesizer*2

*1: The MU181000A or MU181000B is required.

*2: We recommend using the MG3690C series as an external synthesizer.

For details about the MG3690C series, contact Anritsu or our sales representative.

3.2 Inter-Module Connection

Avoid static electricity when handling the devices.

⚠ WARNING

- **When signals are input to this MU183020A/MU183021A, avoid excessive voltage beyond the rating. Otherwise, the circuit may be damaged.**
- **As a countermeasure against static electricity, ground other devices to be connected (including experimental circuits) with ground wires before connecting the I/O connector.**
- **The outer conductor and core of the coaxial cable may become charged as a capacitor. Use any metal to discharge the outer conductor and core before use.**
- **The power supply voltage rating for the mainframe is shown on the rear panel. Be sure to operate the mainframe within the rated voltage range. The mainframe may be damaged if a voltage out of the rating range is applied.**
- **To protect the MU183020A/MU183021A from electrostatic discharge failure, a conductive sheet should be placed onto the workbench, and the operator should wear an electrostatic discharge wrist strap. Always ground the wrist strap to the workbench antistatic mat or the frame ground of the MU183020A/MU183021A.**
- **When removing a cable from a connector on the front panel of the MU183020A/MU183021A, be careful not to add excessive stress to the connector.**
- **Addition of excessive stress to a connector may result in characteristic degradation or a failure. Use a torque wrench (recommended torque: 0.9 N-M) when attaching or removing a cable.**

⚠ CAUTION

Avoid inputting the signal exceeding the maximum input level to the Data Input connector of MU183040A/MU183041A. Failure to do so can cause damage.

Note that the maximum output level of the Data Output connector of MU183020A-x13/x23 and MU183021A-x13 is "3.50 Vp-p" and the maximum input level of the Data Input connector of MU183040A/MU183041A is "2.00 V".

Confirm that the Data Output setting of MU183020A/MU183021A is 2.00 V or less before directly connecting the Data Output connector of MU183020A/MU183021A to the Data Input connector of MU183040A/MU183041A, for example, when checking the operation.

3.2.1 Connecting with MU183040A

This section describes a connection example of MU183020A, MU181000A 12.5GHz synthesizer (hereafter MU181000A), and MU183040A 28G/32G bit/s ED (hereafter MU183040A) that are installed to a mainframe.

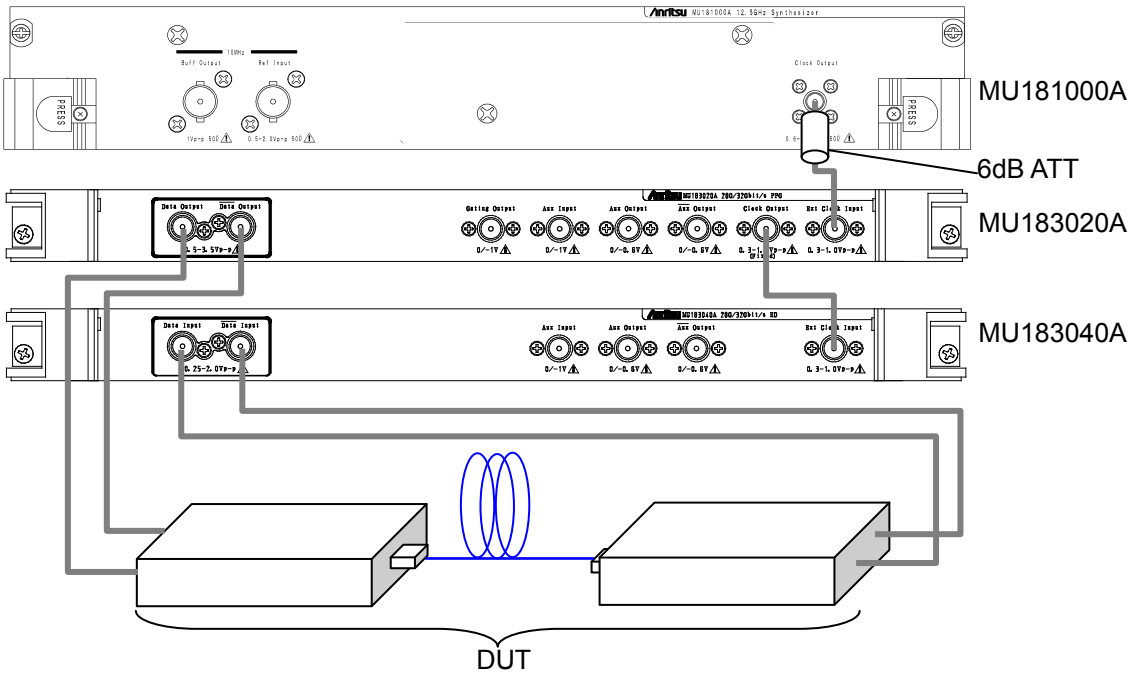


Figure 3.2.1-1 Inter-module connection example

1. For the case of the MU181000A, attach the 6 dB fixed attenuator (ATT) to the Clock Output connector.
   The following models and options do not require the 6dB fixed attenuator.
   MU181000A-x01, MU181000B, MU181000B-x01
2. Connect the Clock Output connector of the MU181000A and the Ext. Clock Input connector of the MU183020A, using a coaxial cable.
3. Connect the Clock Output connector of the MU183020A and the Ext. Clock Input connector of the MU183040A, using a coaxial cable.
4. Connect the Data Output connector of the MU183020A and the Data Input connector of the device under test (DUT) using a coaxial cable. Also connect the $\overline{\text{Data}}$ Output connector of the MU183020A and the $\overline{\text{Data}}$ Input connector of the DUT, using a coaxial cable.
5. Connect the Data Output connector of the DUT and the Data Input connector of the MU183040A, using a coaxial cable. Also connect the $\overline{\text{Data}}$ Output connector of the DUT and the $\overline{\text{Data}}$ Input connector of the MU183040A, using a coaxial cable.
6. Select “Initialize” from the File menu on the menu bar to initialize the entire system.
   Note that all the settings are initialized to the factory default settings by initialization. If necessary, select “Save” from the File menu to save the settings before initialization.

3.2.2 Adding Jitter to Output Signal

MU180000A/B and MU181500B jitter modulation source (hereafter MU181500B) are used to add jitter to signal that is outputted from PPG. Figure 3.2.2-1 shows a connection example of MU181000A, MU181500B, MU183020A, and MU183040A.

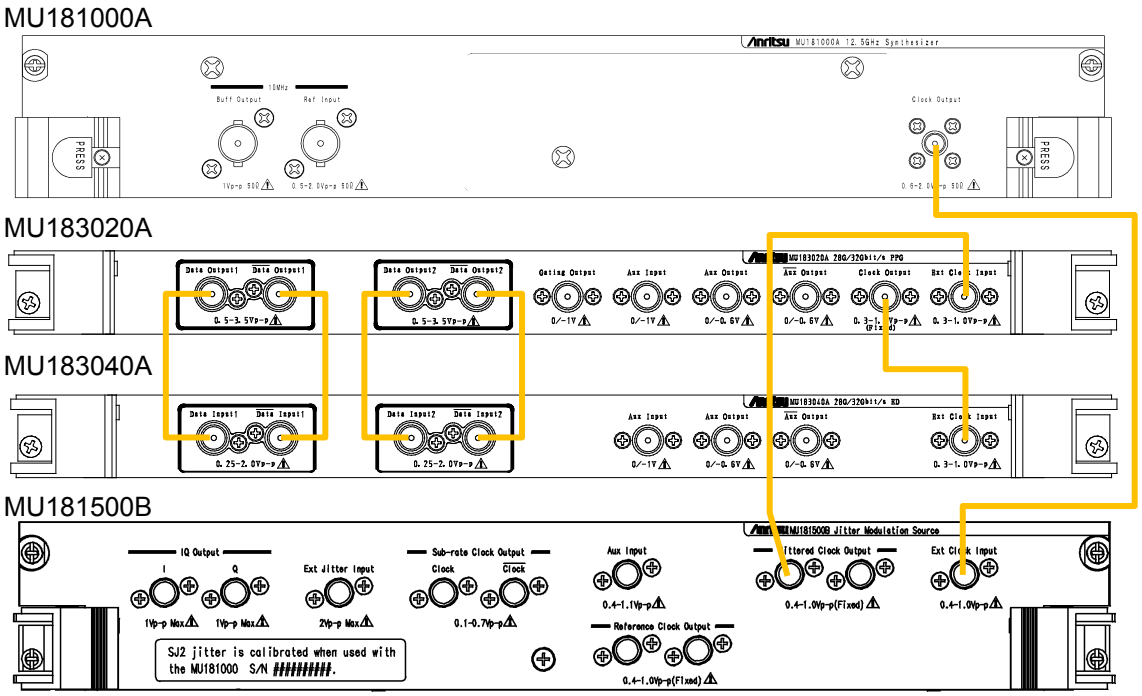


Figure 3.2.2-1 Connection example when adding jitter to output signal

1. Use a coaxial connector to connect the RF Output connector of the MU181000A and the Ext Clock Input connector of the MU181500B.
2. Use a coaxial connector to connect the Jittered Clock Output connector of the MU181500B and the Ext Clock Input connector of the MU183020A.
3. Use a coaxial connector to connect the Clock Output connector of the MU183020A and the Ext Clock Input connector of the MU183040A.
4. Use coaxial cables to connect Data Output and $\overline{\text{Data}}$ Output connectors of the MU183020A with Data Input and $\overline{\text{Data}}$ Input connectors of the MU183040A (2 connections).
5. Select “Initialize” from the File menu on the menu bar to initialize the entire system.
   Note that all the settings are initialized to the factory default settings by initialization. If necessary, select “Save” from the File menu to save the settings before initialization.

3.2.3 Using External Clock

This section describes a connection example of MU183021A, MU183041A, and External Clock. (MU183021A and MU183041A are installed to a mainframe.) MG3692C is used as External Clock in the example.

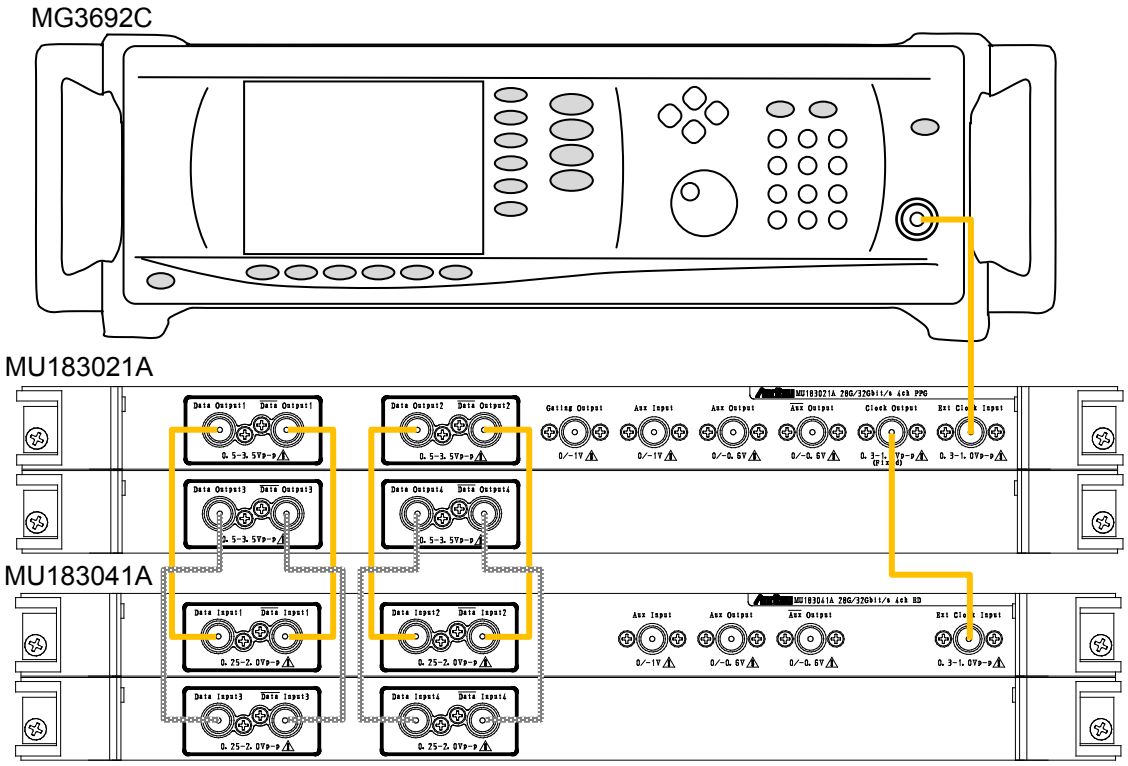


Figure 3.2.3-1 Connection example of External Clock

1. Use a coaxial connector to connect the RF Output connector of the MG3692C and the Ext Clock Input connector of the MU183021A.
2. Use a coaxial connector to connect the Clock Output connector of the MU183021A and the Ext Clock Input connector of the MU183041A.
3. Use coaxial cables to connect Data Output and $\overline{\text{Data}}$ Output connectors of the MU183021A with Data Input and $\overline{\text{Data}}$ Input connectors of the MU183041A (4 connections).
4. Select “Initialize” from the File menu on the menu bar to initialize the entire system.
   Note that all the settings are initialized to the factory default settings by initialization. If necessary, select “Save” from the File menu to save the settings before initialization.

Chapter 4 Configuration of Screens and Tabs

This chapter describes the configuration of the MU183020A screens and tabs.

4.1 Configuration of Entire Setup Dialog Box

Screens have the following configuration if the MU183020A is inserted into a mainframe.

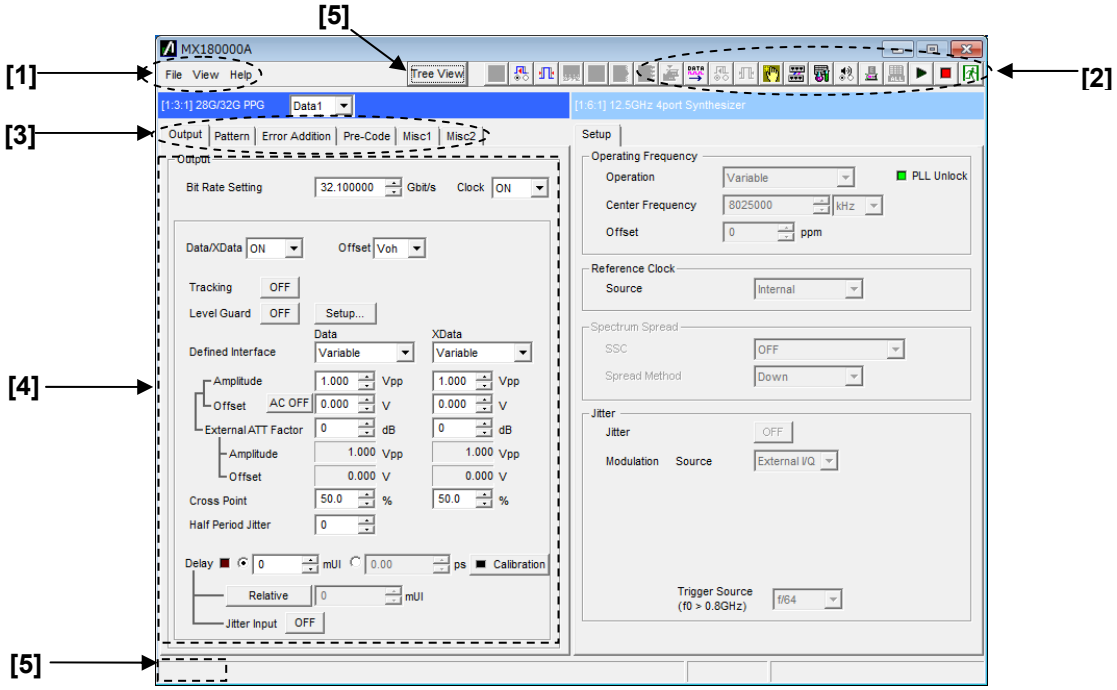


Figure 4.1-1 Screen configuration

The screens consist of four blocks ([1] to [4] in Figure 4.1-1). Table 4.1-1 describes the function of each block.

Table 4.1-1 Function of each block

No.	Block	Function
[1]	Menu bar	Select the setting functions related to the entire device.
[2]	Module function buttons	Shortcut buttons for the function items specific to the displayed module. Click on the Menu bar > View > Button Menu. Up to 17 function buttons can be selected and displayed.  For the user customize screen of buttons, refer to 4.3 "User Customize Dialog".
[3]	Function setting selection tabs	Click to switch the module operation tab window according to the function items. Refer to Chapter 5 “Operation Method” for details.
[4]	Operation window	Configures settings specific to each module. Refer to Chapter 5 “Operation Method” for details.
[5]	Tree View Display Button Display Area	Clicking the button can display the Tree View screen. Also, moving the cursor over the bottom left area can display the Tree View screen.

4.2 Operation Tab Windows

Tabs to operate the MU183020A have the following functions.
Refer to Chapter 5 “Operation Method” for details on each tab.

Figure 4.2-1 Tabs

Table 4.2-1 Function of each tab

Tab	Function
Output	Selection and setting of Data/XData and Clock outputs Various output interface settings can be configured in this tab window.
Pattern	Selection and setting of test pattern A test pattern can be selected and edited in this tab window.
Error Addition	Selection and setting of error addition The error addition function can be set in this tab window.
Pre-Code	This tab is displayed when Combination is selected in the Misc2 tab of MU183020A-x22/x23 or MU183021A.
Misc1	Other settings Pattern generation method setting, auxiliary input/output selection, and other settings can be configured in this tab window.
Misc2	Setting of frequency ratio of Clock Input and Data Output and Channel Combination between channels.

4.3 User Customize Dialog

On the User Customize Dialog, main parameters of multiple modules can be displayed and set. The figure below shows a dialog displaying some parameters of the MU183020A, MU183040B, and MU181500B as an example. Additionally, parameters of a module that is not installed in the MP1800A cannot be set.

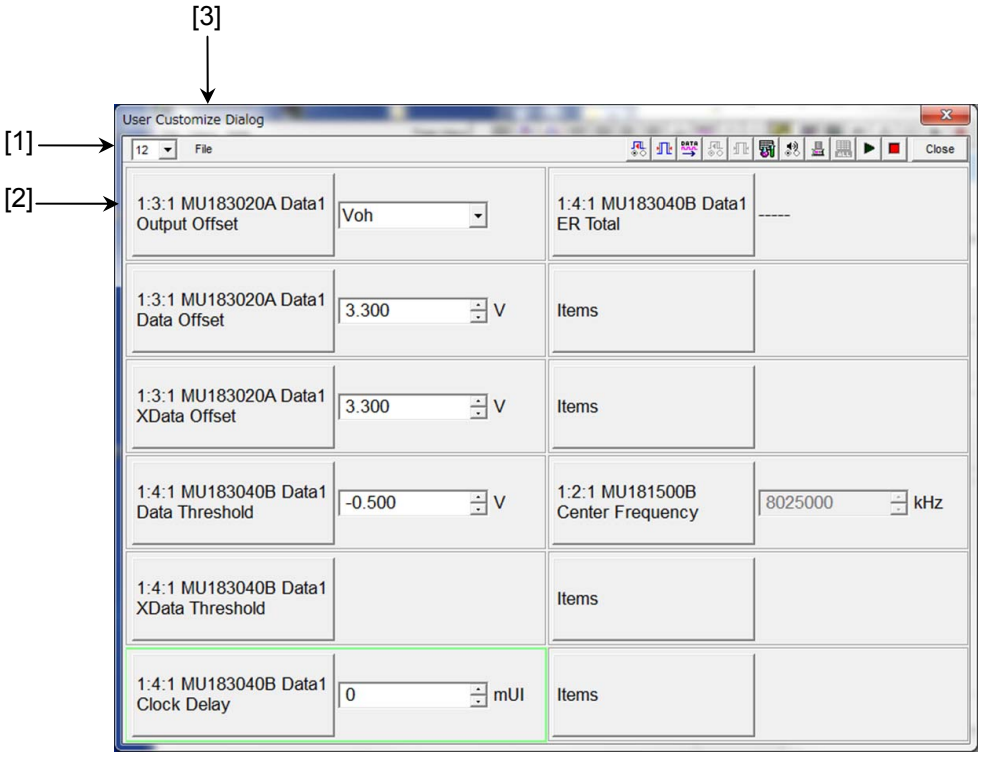


Figure 4.3-1 User Customize Dialog

[1] Number of parameters displayed
Select 6 or 12 or 18.

[2] Selection of custom items
Select a desired module and parameter. For example, to select Data1 Data Offset of MU183020A 32Gbit/s PPG of Unit1, Slot3, and Port1, first select the desired module 1:3:1 MU183020A and then the parameter Data1 Data Offset.

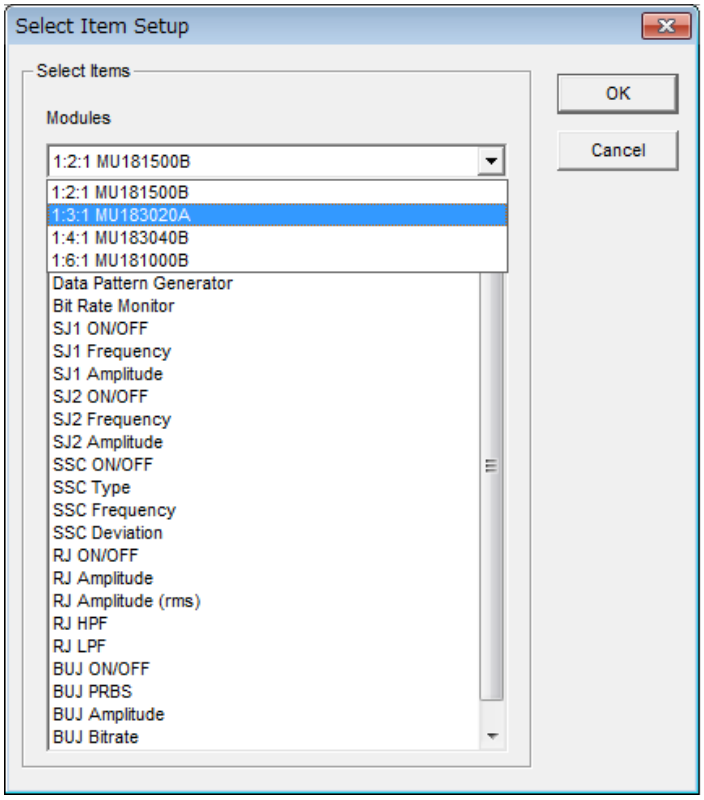


Figure 4.3-2 Selecting Module

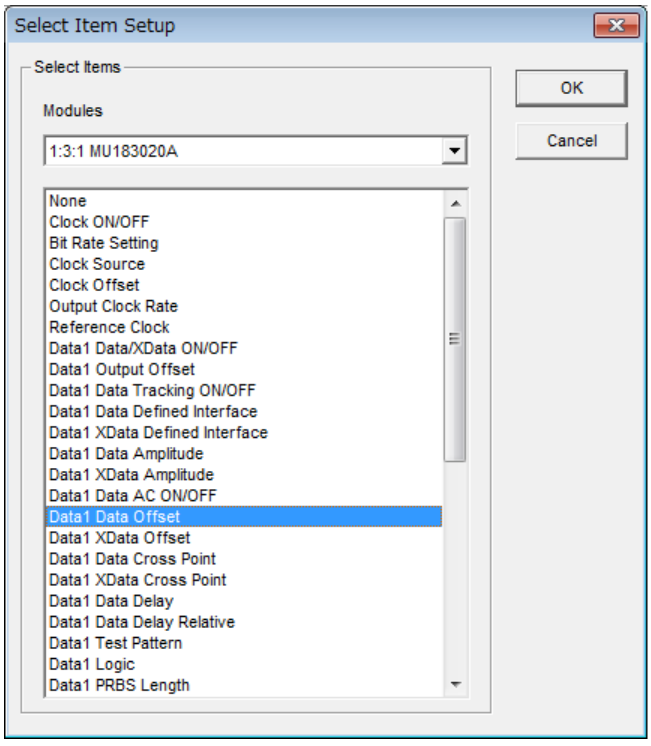


Figure 4.3-3 Selecting Parameter

[3] File Menu

Saves and reads the customize dialog setup. The customize dialog setup file can be saved and read by the extension (.UCD). Additionally, the 32G systems (MU183020A, MU183040B, MU181500B, and MU181000B) can load a preset file (.UCP) of frequently used functions.

Chapter 5 Operation Method

This chapter describes the functions provided in the function setting selection tabs on the MU183020A/MU183021A operation window.

5.1 Setting Output Interface

To set the output interface, click the **Output** tab of the operation window. On the **Output** tab, the settings for the Data, XData, and Clock can be configured.

The Data signal is output from the Data connector of the MU183020A/MU183021A, and the XData signal is output from the $\overline{\text{Data}}$ connector. Also, the Clock signal is output from the Clock connector. Hereinafter, the settings for the $\overline{\text{Data}}$ connectors are described as the settings for XData respectively.

5.1.1 Setting the data

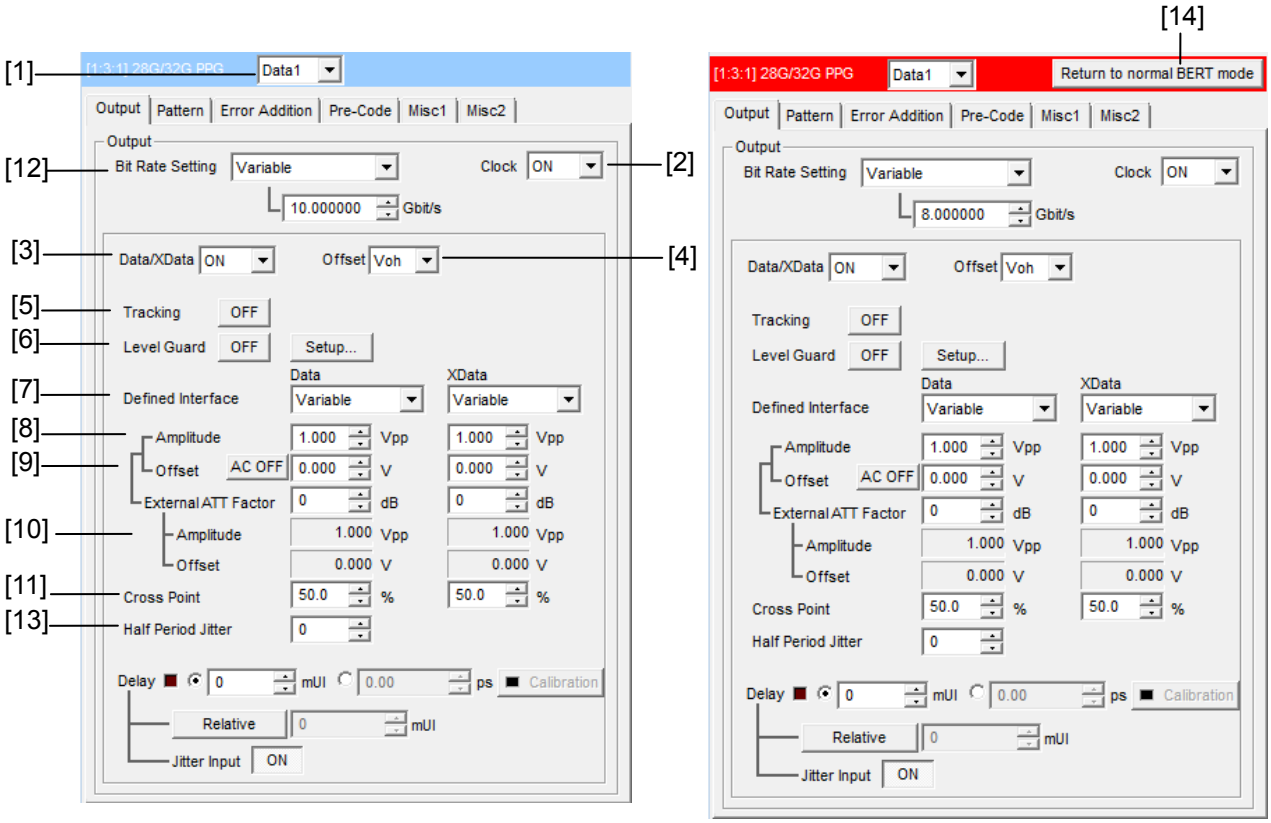


Figure 5.1.1-1 Output Tab When Setting the Data

Delay appears when the option x30 or x31 is added.

[1] From the drop-down list, select a channel you want to set the data.

[2] Set Clock Output ON/OFF.

Note:

Even if Clock output is set to OFF, a few tens mV clock signal may be outputted depending on operation bit rate.

[3] Set Data/XData Output ON/OFF.
This setting applies to the selected MU183020A/MU183021A. When enabling the output signal (ON), enabling the output of all the instruments, by clicking the Output module function button on the menu bar, is also required.

Notes:

- The DUT may be damaged if the output setting is configured incorrectly. To prevent damage to the DUT, confirming the interface condition with the DUT, or configuring the level guard setting before making the output setting is recommended.

- When PCML, LVPECL, or NECL is selected for Defined Interface, the voltage corresponding to the DUT's termination voltage is applied to the output side of the MU183020A/MU183021A. In this event, the DUT may be damaged if the interface conditions do not match. Be sure to confirm the interface conditions.

- Waveforms may be distorted (what is known as a ringing phenomenon) when a commercially-available ECL terminator is used to observe output waveforms. This is, however, caused by the characteristics of the ECL terminator; the waveform output from the mainframe is not distorted.

- The current for the output part is limited (50 mA for sourcing current and 80 mA for sinking current) for protection. If an overcurrent flows due to the wrong interface condition, the offset voltage for an observed waveform may therefore not reach the set level.

- Be sure to confirm that a fixed attenuator is connected between the MU183020A/MU183021A and the DUT before setting the external ATT factor. If the external ATT factor is set when no fixed attenuator is connected or when the fixed attenuator has an attenuation value less than that set in the External ATT Factor area, the DUT may be damaged.

[4] Select the offset reference from the drop-down list.
The setting range for the offset and amplitude is restricted by each setting value. Refer to Appendix C "Setting Restrictions" for details on the setting ranges for the offset and amplitude. When the offset reference is changed, the offset value is calculated and changed based on the changed offset reference.

Table 5.1.1-1 Offset reference

Offset reference	Description
Voh	The offset value is set based on the high level.
Vth	The offset value is set based on the center level between the high and low levels.
Vol	The offset value is set based on the low level.

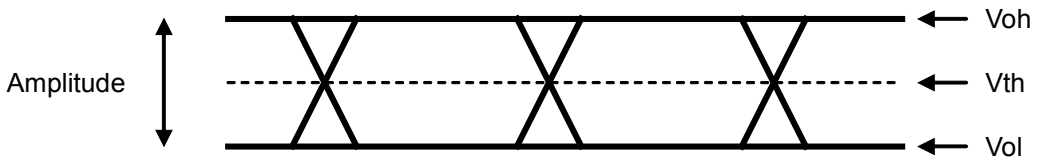


Figure 5.1.1-2 Setting offset

[5] Set Tracking ON/OFF.
When Tracking is set to ON, the settings for the XData become the same as those for the Data.

[6] Configure the level guard settings.
Click [Setup] to open the setup dialog box, and set the maximum amplitude (Amplitude), maximum offset (Offset Max (Voh); maximum value of the offset high level), and minimum offset (Offset Min (Vol); minimum value of the offset low level) for level guard, so that an excessively high voltage is not applied to the DUT.

When the external ATT factor is set (see [10] below), the level guard settings (Amplitude, Offset Max (Voh), and Offset Min (Vol)) after passing through the fixed attenuator, which is connected between the MU183020A/MU183021A and the DUT, limit the output level of these setting value. Therefore, if you use the fixed attenuator without connecting, a signal exceeding the setting value is output.

[7] Separately configure the defined interface setting for Data and XData.
Note that it may not be possible to select some items, depending on the level guard setting.

Table 5.1.1-2 Amplitude setting values

Item	Amplitude		Offset Vth	Options
	Voh	Vol		
Variable	–	–	–	x12/x13/x22/x23
PCML	+3.3 V	+2.8 V	+3.05 V	x12/x13/x22/x23
NCML	0.0 V	–0.5 V	–0.25 V	x12/x13/x22/x23
SCFL	0.0 V	–0.9 V	–0.45 V	x12/x13/x22/x23
NECL	–0.9 V	–1.7 V	–1.3 V	x12/x13/x22/x23
LVPECL	+2.4 V	+1.6 V	+2.0 V	x12/x13/x22/x23

[8] Separately set the amplitude for Data and XData.
The setting range varies depending on the level guard setting, offset setting, and installed option. The amplitude setting ranges when Defined Interface is set to Variable are shown in the table below.

Table 5.1.1-3 Amplitude setting range

Installed Option	Amplitude	Resolution
x12 or x22	0.5 to 2.0 Vp-p	0.002 V
x13 or x23	0.5 to 3.5 Vp-p	0.002 V

Note:

Options x22 and x23 are supported only by the MU183020A.

[9] Separately set the offset for Data and XData.

Offset can be set within the range from –2.000 to +3.300 V in 0.001 V steps (when reference level is Voh). Clicking to change [AC OFF] to [AC ON] enables AC-coupled output. The lower-band cutoff frequency is about 10 kHz.

[10] Separately set the external ATT factor for Data and XData.
When a fixed attenuator is connected to the Data/XData output connector of the MU183020A, the attenuation of the attenuator is added to the value for the DUT and displayed. A value from 0 to 40 dB can be set in 1-dB steps. When Defined Interface is not set to other than Variable, the setting is reset to 0 and becomes invalid. Values displayed in the External ATT Factor-Amplitude and Offset display areas indicates the amplitude and offset value after passing through the attenuator, respectively.

[11] Separately set the cross point setting for Data and XData.
The setting range varies depending on the installed option.

Table 5.1.1-4 Cross point setting range

Installed Option	Data/XData independency	Cross point setting range	Resolution
x12 or x22	Independent	20.0 to 80.0% (Amplitude 1 to 2.0V) 30.0 to 70.0% (Amplitude 0.500 to 0.998V)	0.1%
x13 or x23	Independent	20.0 to 80.0% (Amplitude 1 to 3.5V) 30.0 to 70.0% (Amplitude 0.500 to 0.998V)	0.1%

Note:

Options x22 and x23 are supported only by the MU183020A.

[12] When the clock source is [External], the bit rate of data is displayed.

When the clock source is MU181000A, MU181000B or MU181500B, you can set the bit rate of data.

For details, refer to 5.1.4 “Setting bit rate" and 5.6.1 “Setting clock”.

[13] Set the Half Period Jitter for the data output signal. The Cross Point time axis can be adjusted as shown in Figure 5.1.1-3 using this setting while observing the Eye pattern. Adjacent Eye patterns become equal at default 0.

Table 5.1.1-5 Half Period Jitter setting range

Setting values	Resolution
–20 to 20	1

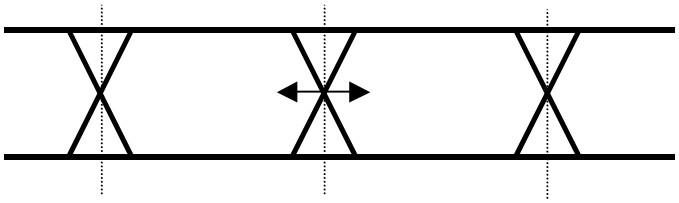


Figure 5.1.1-3 Setting Half Period Jitter

[14] This button is displayed only when the MX180000A is connected to the MX183000A High Speed Serial Data Test Software. For details, refer to below.

☞ 4.3.3 “Move to special mode for compliance test” in the *MX183000A High Speed Serial Data Test Software Operation Manual*.

5.1.2 Setting the delay

The Data output phase can vary relative to the Clock output when any of the following is installed:

- MU183020A-x30
- MU183020A-x31
- MU183021A-x30.

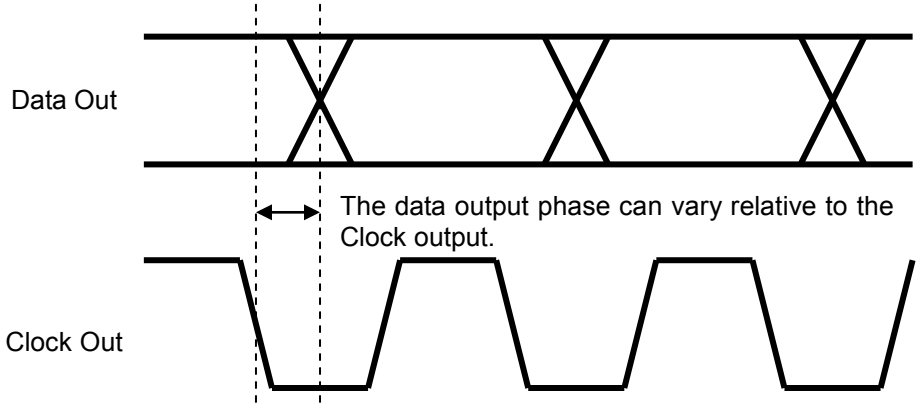


Figure 5.1.2-1 Delay setting

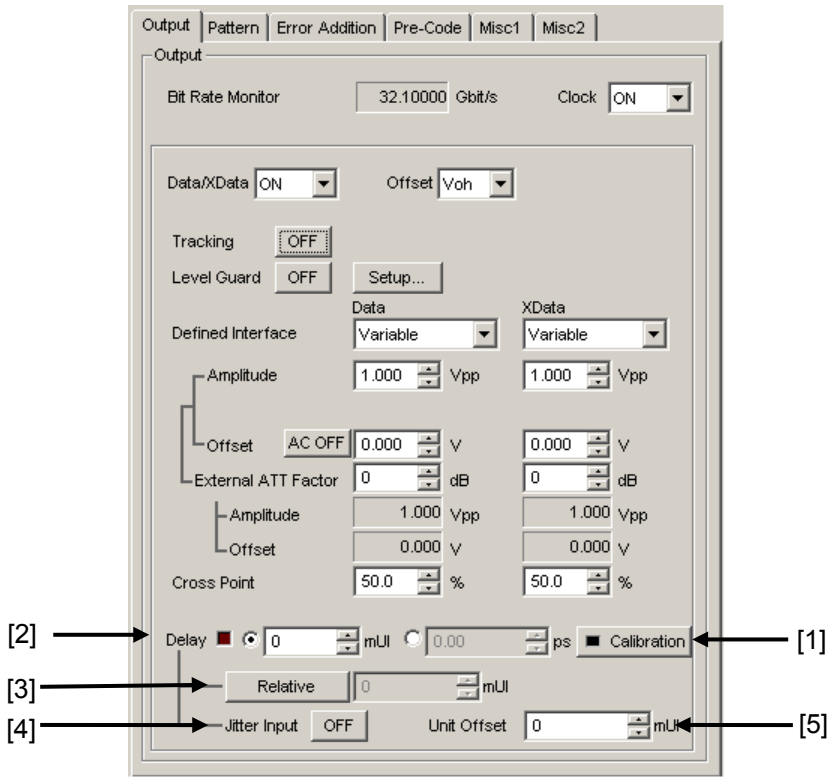


Figure 5.1.2-2 Output Tab When Setting the Delay

[1] Click [Calibration] to perform calibration of a phase variable function. When the power is supplied, the frequency is changed, or the ambient temperature fluctuates, the calibration prompting alarm LED lights up. In such a case, click this button to perform calibration. Calibration will finish within 1 second.

[2] Set the delay in mUI or ps units.

<In the case of mUI units>

The delay can be set from –1000 to 1000 mUI, in 2-mUI steps. When the 2 ch Combination, 4ch Combination, or Channel Synchronization Option is installed, setting is supported from –64,000 to 64,000 mUI in 2-mUI steps.

<In the case of ps units>

The delay can be set in steps of ps units, equivalent to 2 mUI. The setting range is the range converting –1000 to 1000 mUI in ps units. During 2ch Combination, 4ch Combination or Channel Synchronization, the setting range is equivalent to the range when the unit is mUI (–64,000 to 64,000 mUI), converted into ps units. Example:

Table 5.1.2-1 Delay setting range

Bit rate	Setting range	
	Normal	2ch Combination 4ch Combination Channel Synchronization
32.1 Gbit/s	–31.14 to 31.14 ps	–1 993.74 to 1 993.74 ps
25 Gbit/s	–40 to 40 ps	–2 560 to 2 560 ps
2.4 Gbit/s	–416 to 416 ps	–26 665.6 to 26 665.6 ps

[3] Click [Relative] to use the current set phase value as the reference of relative 0 for delay setting.

[4] Set the Jitter Input.
When inputting jitter-modulated clocks, set Jitter Input of Delay to ON.

[5] Set the Delay offset for each main frame (MP1800A or MT1810A). This box is available only when the Unit Sync setting is ON. The setting is the same for all MU183020A/21A modules installed in the same main frame.

Set a value between –1000 and +1000 mUI in 2-mUI steps.
A value between –128,000 and +128,000 can be set in 2-mUI steps for Combination and Channel Synchronization.

However, due to the restrictions of the Delay setting in item [2], the setting range is as below.

Delay Setting + Unit Offset Setting = ±1000mUI (or ±128,000 mUI).

For how to use this function, refer to Appendix E "Preparing to Use Unit Sync Function".

Notes:

- When the frequency or the temperature condition is changed, the LED on the [Calibration] lights, prompting performance of calibration. If calibration is not performed at this time, the error in the phase setting may be greater than at a normal phase setting.

- Values displayed in ps units vary as the frequency changes, because the MU183020A sets phases in mUI units as an internal standard.

Delay setting in the case of Combination or CH Synchronization

In the case of Combination or Channel Synchronization when multiple MU183020A or MU183021A modules are mounted, the delay between two or more channels can be changed relatively, as shown in following figure.

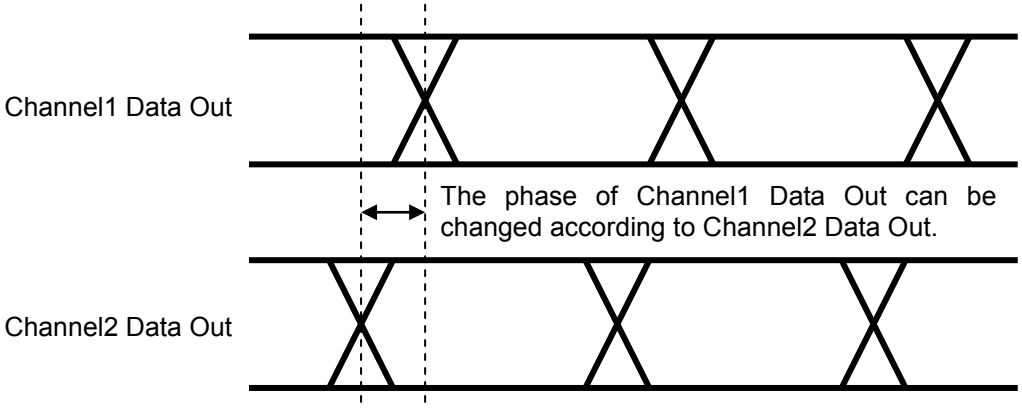


Figure 5.1.2-3 Delay setting in the case of Combination

5.1.3 When setting jitter-modulated signals

- When inputting jitter-modulated clocks, use MU181000A/B and MU181500B. For inter-module connection, refer to 3.2.2 “Adding Jitter to Output Signal”.
- Set Jitter Input of Delay to ON.
- Set the jitter modulation for input signals to non-modulation when executing calibration of Delay.
- When configuring Combination Setting, set the jitter modulation to non- modulation before setting Combination or Channel Synchronization.
- When changing the input frequency while Combination or Channel Synchronization is set, be sure to set Jitter Input of Delay for the MU183020A to ON and then set the jitter modulation to ON, in this order, after changing the frequency for measurement.

Figure 5.1.3-1 Delay Setting Items in the Output Tab (Closeup)

Notes:

- When jitter-modulated clock is input while Jitter Input of Delay is set to OFF, the phase may become unstable.
- The Delay lamp may light up when a jitter-modulated clock signal is input. In addition, phase setting error may increase.

5.1.4 Setting bit rate

When the clock source is MU181000A/B or MU181500B, the bit rate of data output can be set. For how to set the clock source, refer to 5.6.1 “Setting clock”.

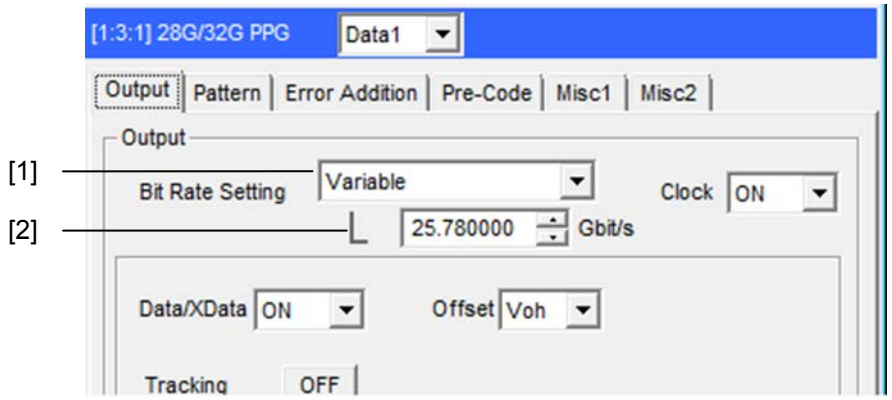


Figure 5.1.4-1 [Output] Tab Bit Rate Setting Area

[1] When the clock source is MU181000A, MU181000B or MU181500B, select a bit rate from the preset standard list (table below) or set to [Variable] to specify an arbitrary value.

[2] A corresponding bit rate is displayed when a preset standard is selected. When set to [Variable], an arbitrary bit rate can be specified.

Note:

A bit rate can be set only when the MU181500B clock source is MU181000A or MU181000B. When using an external clock source for MU181500B, the PPG bit rate cannot be set.

Table 5.1.4-1 Preset Standard of Bit Rate

Preset Standard	Bit rate [Gbit/s]
100G ULH	32.100 000*1
32G FC	28.050 000
100G OTU4	28.000 000
100GbE(25.78x4)	25.781 250*2
Infiniband EDR	25.781 250*2
SAS	24.000 000
PCI Express Gen4	16.000 000
Infiniband FDR	14.062 500
16G FC	14.025 000
10GFC over FEC	11.316 800
10GbE over FEC	11.095 700
OTU2	10.709 225*2
G975 FEC	10.664 228*2
10G FC	10.518 750
10GbE	10.312 500
USB3.1	10.000 000
Infiniband QDR	10.000 000
OC-192/STM-64	9.953 280
8G FC	8.500 000
PCI Express Gen3	8.000 000
PCI Express Gen2	5.000 000
USB3.0	5.000 000
PCI Express Gen1	2.500 000

*1: Only when the Option x01 is installed.

*2: The bit rate resolution is automatically set to 0.000002 Gbit/s or 0.000004 Gbit/s interlinking with the output clock rate of the 32G PPG Misc2 and the current bit rate. Thus, the bit rate may not be set to the exact standard value.

Table 5.1.4-2 Bit Rate Setting Range for [Variable]

Preset Standard	Bit rate [Gbit/s]
Variable	2.400 000 to 28.100 000 Gbit/s (32.100 000Gbit/s with Option x01 installed) Can be set in increments of 0.000 001Gbit/s. *

*: When it cannot be set by the Output Clock Rate set for the interlinked 32G PPG Misc2 and the current bit rate, the bit rate resolution is set to 0.000002 Gbit/s or 0.000004 Gbit/s.

5.2 Setting Test Patterns

On the **Pattern** tab, you can set test pattern.

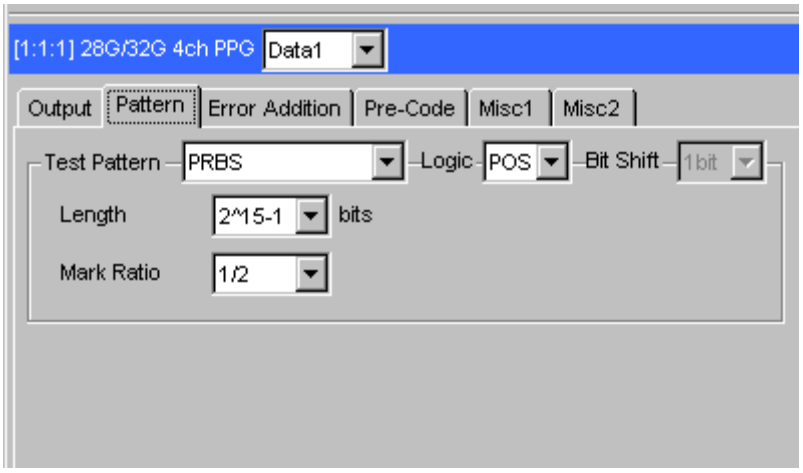


Figure 5.2-1 Pattern tab

5.2.1 Test Pattern type

The following four test patterns can be selected.

- PRBS
- Zero-Substitution
- Data
- Mixed

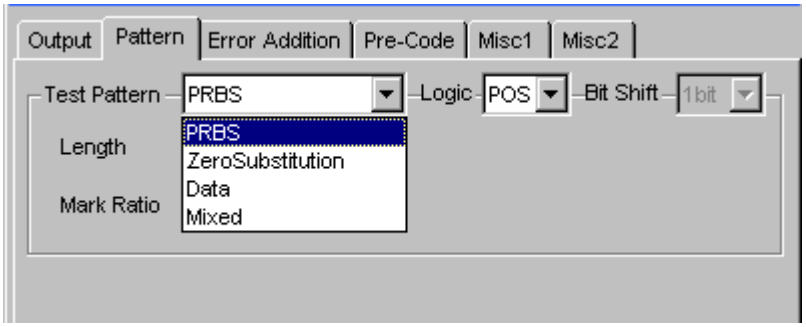


Figure 5.2.1-1 Selecting test pattern

How to set each test pattern is described in the subsequent sections.

5.2.2 Setting PRBS pattern

This section describes how to set the parameters required when PRBS is selected as the test pattern.

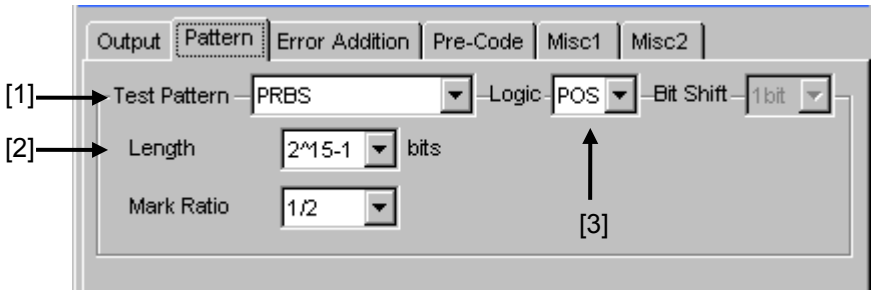


Figure 5.2.2-1 Setting items for PRBS pattern

[1] Select "PRBS" from the Test Pattern drop-down list.

[2] Set the number of the PRBS pattern stages.
Set the PRBS pattern length in the format of 2^n-1 (n = 7, 9, 10, 11, 15, 20, 23, 31).

[3] Set the logic of the test pattern.

Table 5.2.2-1 Test pattern logic setting

Setting	Description
POS (positive logic)	The high level of a signal is defined as "0".
NEG (negative logic)	The high level of a signal is defined as "1".

Refer to Appendix A "Pseudo-Random Pattern" for the PRBS pattern generation principle.

5.2.3 Setting Zero-substitution pattern

This section describes how to set the parameters required when Zero-Substitution is selected as the test pattern.

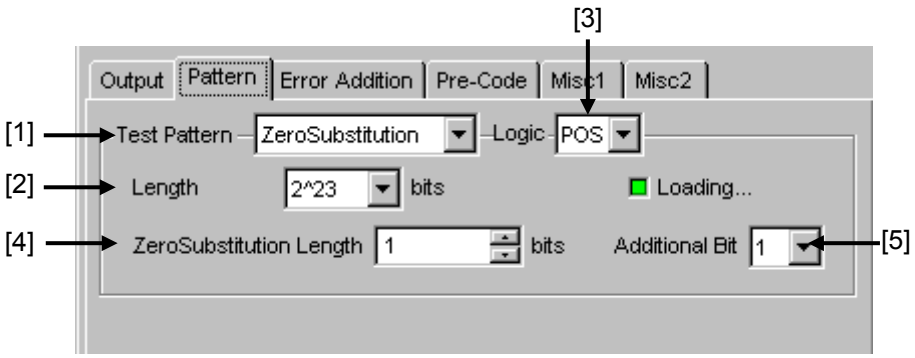


Figure 5.2.3-1 Setting items for ZeroSubstitution pattern

[1] Select "Zero Substitution" from the Test Pattern drop-down list. Test pattern loading starts and the "Loading…" LED lights.

[2] Set the configuration (number of stages) of the zero-insertion pattern test signal.

Select either of the following test pattern signals.
2^n (n = 7, 9, 10, 11, 15, 20, or 23) [Compatible with the existing models]
2^n-1 (n = 7, 9, 10, 11, 15, 20, or 23) [Pure PRBS signal]

[3] Set the logic of the test pattern.

Table 5.2.3-1 Test pattern logic setting

Setting	Description
POS (positive logic)	The high level of a signal is defined as "1".
NEG (negative logic)	The high level of a signal is defined as "0".

[4] Set the number of 0-insertion (substitution) bits in the zero-insertion (substitution) pattern.

The number of available 0-insertion bits varies depending on the pattern test signal selected from the Length drop-down list ([2] in Figure 5.2.3-1) as follows.

(a) When 2^n-1 is set for Length: 1 to 2^n-2, in 1-bit steps

(b) When 2^n is set for Length: 1 to 2^n-1, in 1-bit steps

[5] Set the final bit of the zero-insertion pattern.
Note that this setting is invalid when Length is set to 2^n–1.

Table 5.2.3-2 Setting of last bit of zero-insertion pattern

Setting	Description
1	The 2^nth bit is set to "1" (compatible with the existing models).
0	In order to make an M-series signal, 1 bit of "0" is added to the last of consecutive 0 strings to configure a zero-insertion pattern.

Notes:

The following data patterns may cause decrease in data output amplitude by about 50%:

- Data pattern in about a 5 µs period after:
  continuing "0" for 5 µs or more due to "0" insertion
  or
  continuing "0" (or "1") for 5 µs or more due to such as burst pattern

- Pattern with the mark ratio other than 1/2.

If the MU183040A/41A receives this data signal, then there may be disagreement between the optimal threshold voltage and the offset voltage (Vth) that is set for the MU183020A/21A.

In this case, an error can occur, so use such as an oscilloscope to check a data signal, and then adjust threshold voltage.

5.2.4 Setting Data pattern

This section describes how to set the parameters required when Data is selected as the test pattern.

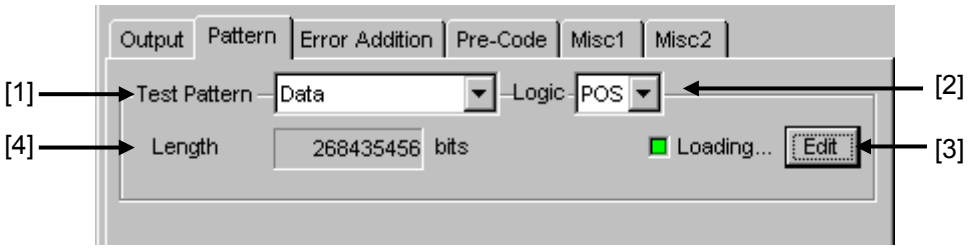


Figure 5.2.4-1 Setting items for Data pattern

[1] Select "Data" from the Test Pattern drop-down list.
Test pattern loading starts and the "Loading…" LED lights.

[2] Set the logic of the test pattern.

Table 5.2.4-1 Test pattern logic setting

Setting	Description
POS (positive logic)	The high level of a signal is defined as "1".
NEG (negative logic)	The high level of a signal is defined as "0".

[3] Click [Edit] to open the **Pattern Editor** dialog box in which test patterns can be edited.
When editing of a test pattern is finished, click [OK] to close the **Pattern Editor** dialog box. The edited test pattern is then loaded to the hardware. The "Loading…" LED lights during Data pattern loading. Refer to Section 5.2.6 "Editing test pattern in Pattern Editor dialog box" for details on how to edit test patterns in the **Pattern Editor** dialog box.

[4] The length of the test pattern data currently set is displayed.

Notes:

- It may take a long time to load a test pattern when the data length is long.

  Refer to the following reference loading time values, for the cases where the data length is set to maximum. These values are only references and do not guarantee the Loading time.

  Maximum loading time for 1ch: About 3 min.
  Maximum loading time for 2ch: About 6 min.
  Maximum loading time for 4ch: About 12 min.

- The following data patterns may cause decrease in data output amplitude by about 50%:

  - Data pattern in about a 5 μs period after :
    "0" insertion
    or
    continuing "0" (or "1") for 5 μs or more due to such as burst pattern

  - Pattern with the mark ratio other than 1/2.

  If the MU183040A/41A receives this data signal, then there may be disagreement between the optimal threshold voltage and the offset voltage (Vth) that is set for the MU183020A/21A.

  In this case, an error can occur, so use such as an oscilloscope to check a data signal, and then adjust threshold voltage.

- When the Test Pattern is Data or Mixed, if the MU183040A/41A receives a signal that is a combined signal of "PRBS pattern after continuous **0** bits (shown in Note 2)" and "PRBS pattern after continuous **1** bits", then the optimum threshold voltages of them are each different. Due to this difference, bit errors in all patterns may not be measured.

5.2.5 Setting Mixed pattern

When "Mixed" is selected, a block consisting of programmable test patterns and PRBS patterns can be set.

A programmable test pattern added with a PRBS pattern is defined as "row", one block is composed of two or more rows. A mixed data test pattern is set by configuring multiple blocks.

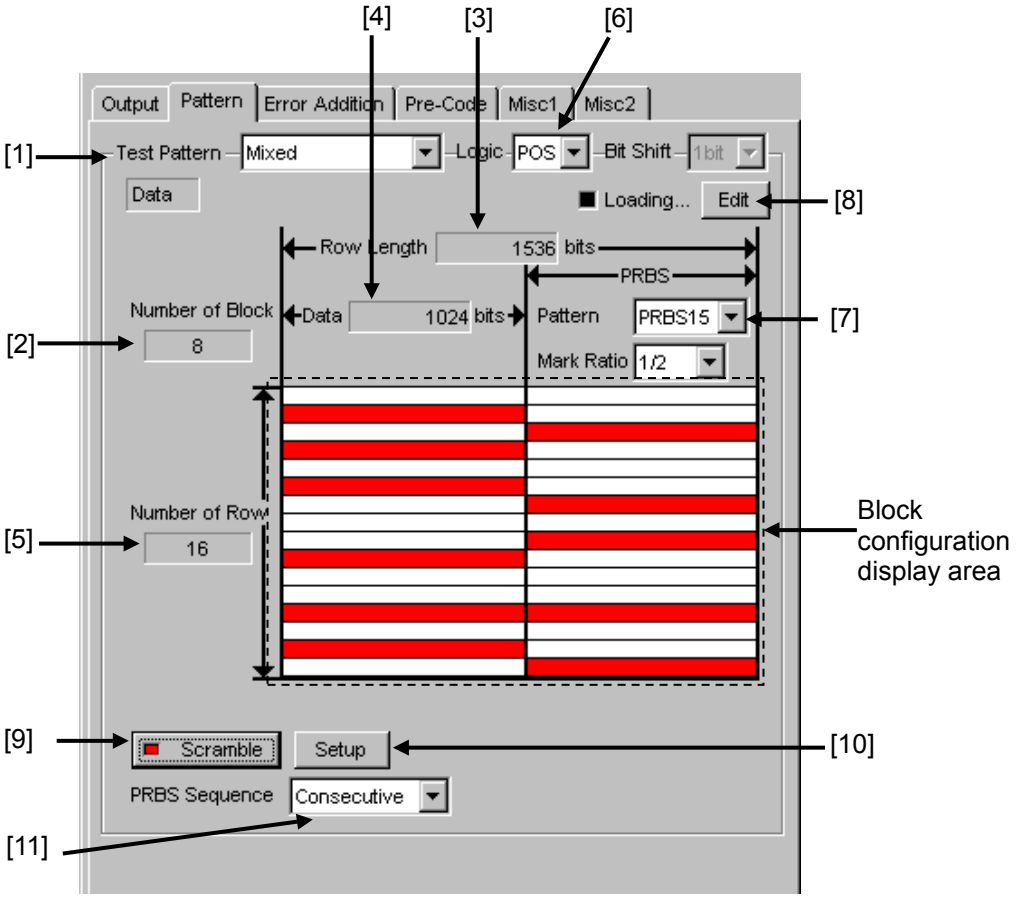


Figure 5.2.5-1 Setting items for Mixed Data pattern

[1] Select "Mixed" from the Test Pattern drop-down list.

[2] The number of all blocks in the pattern data edited in the **Pattern Editor** dialog box is displayed. The maximum number of blocks is 511.

[3] The length of 1 row of the pattern data edited in the **Pattern Editor** dialog box is displayed.

[4] The length of the Data pattern edited in the **Pattern Editor** dialog box is displayed.

[5] The number of rows in one block of the pattern data edited in the **Pattern Editor** dialog box is displayed.

[6] Set the logic of the test pattern.

Table 5.2.5-1 Test pattern logic setting

Setting	Description
POS (positive logic)	The high level of a signal is defined as "1".
NEG (negative logic)	The high level of a signal is defined as "0".

[7] Set the number of the PRBS pattern stages.
Set the PRBS pattern length in the format of 2^n-1 (n = 7, 9, 10, 11, 15, 20, 23, 31).

[8] Click [Edit] to open the **Pattern Editor** dialog box in which test patterns can be edited.
When editing of a test pattern is finished, click [OK] to close the **Pattern Editor** dialog box. The edited test pattern is then loaded to the hardware. The "Loading…" LED lights during test pattern loading. Refer to Section 5.2.6 "Editing test pattern in Pattern Editor dialog box" for details on how to edit test patterns in the **Pattern Editor** dialog box.

Notes:

- It may take a long time to load a test pattern when the data length is long.

  Refer to the following reference loading time values, for the cases where the data length is set to maximum. These values are only references and do not guarantee the Loading time.

  Maximum loading time for 1ch: About 3 min.
  Maximum loading time for 2ch: About 6 min.
  Maximum loading time for 4ch: About 12 min.

- The following data patterns may cause decrease in data output amplitude by about 50%:

  - Data pattern in about a 5 μs period after :
    "0" insertion
    or
    continuing "0" (or "1") for 5 μs or more due to such as burst pattern

  - Pattern with the mark ratio other than 1/2.

  If the MU183040A/41A receives this data signal, then there may be disagreement between the optimal threshold voltage and the offset voltage (Vth) that is set for the MU183020A/21A.

In this case, an error can occur, so use such as an oscilloscope to check a data signal, and then adjust threshold voltage.

- When the Test Pattern is Data or Mixed, if the MU183040A/41A receives a signal that is a combined signal of "PRBS pattern after continuous **0** bits (shown in Note 2)" and "PRBS pattern after continuous **1** bits", then the optimum threshold voltages of them are each different. Due to this difference, bit errors in all patterns may not be measured.

[9] Set scramble ON/OFF.

PRBS7 scramble can be executed for the part of the test pattern. When [Scramble] is clicked while the LED on the button is off, the LED lights and scramble is executed for the output signal. The scramble area set from the [Setup] is displayed red in the block configuration display area.
When [Scramble] is clicked while the LED on the button is on, the LED goes off and scramble for the output signal is stopped.

[10] Configure the scramble settings.

Click [Setup] to open the **Scramble Setup** dialog box. Select the check box for the target area for scramble. After selecting the target area(s), click [OK].

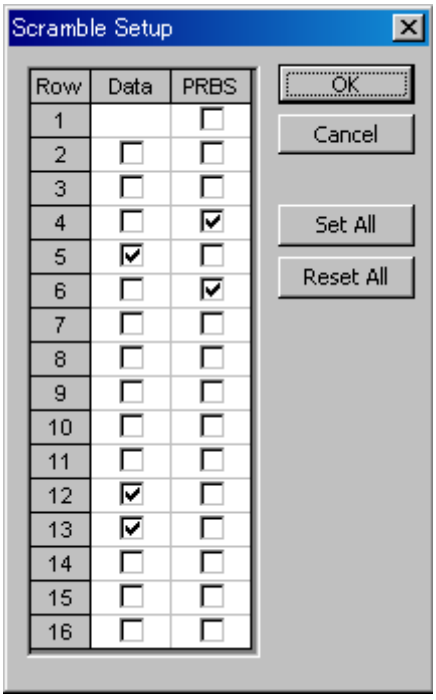


Figure 5.2.5-2 Scramble Setup dialog box

Note:

Scramble cannot be set for the data area of the first row in each block.

[11] Set the PRBS signal generation method.
Set the continuity of the PRBS pattern strings in a Mixed pattern.

Table 5.2.5-2 PRBS signal generation method setting

Setting	Description
Restart	The end of the PRBS of the specified last block and the start of the PRBS of the next subsequent block are not continuous.
Consecutive	The end of the PRBS of the specified last block and the start of the PRBS of the next subsequent block are not continuous.

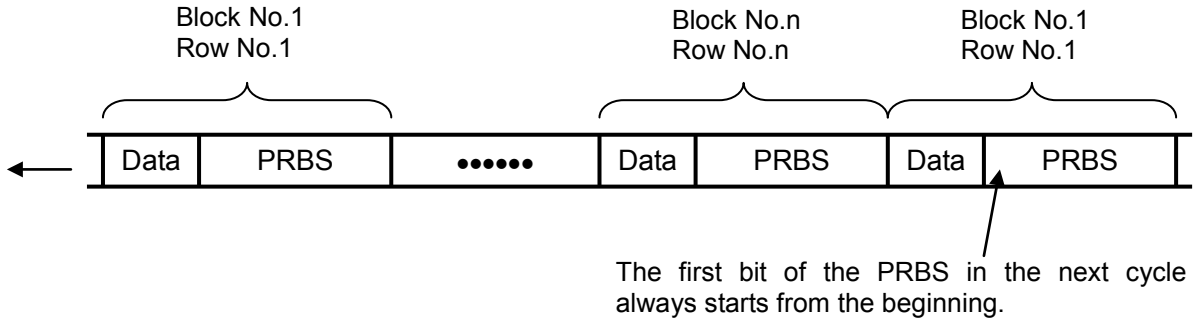


Figure 5.2.5-3 Continuity of PRBS pattern strings (Restart)

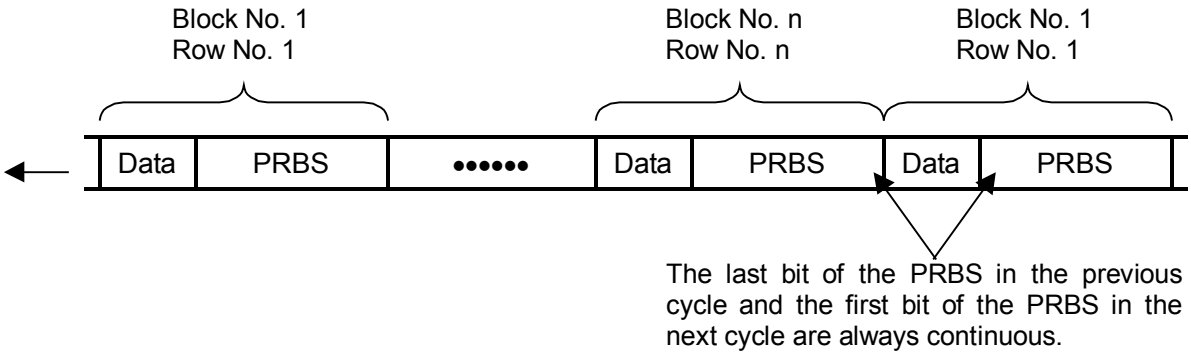


Figure 5.2.5-4 Continuity of PRBS pattern strings (Consecutive)

5.2.6 Editing test pattern in Pattern Editor dialog box

This section describes how to edit test patterns with the following patterns selected on the **Pattern** tab.

- Data
- Mixed

5.2.6.1 Common setting items

The **Pattern Editor** dialog box is displayed when [Edit] is clicked.

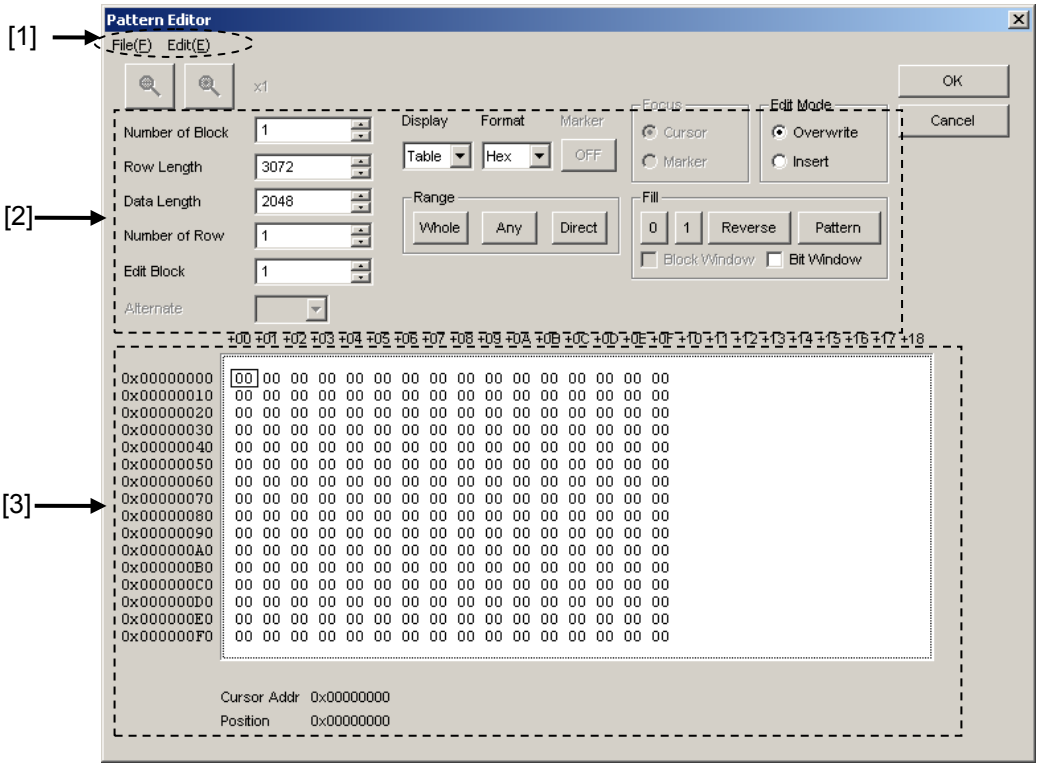


Figure 5.2.6.1-1 Pattern Editor dialog box

[1] Menu items on menu bar

Table 5.2.6.1-1 Menu bar configuration

Menu	Menu item	Description
File	Open	Opens a setting file saved in the binary pattern (Binary Pattern), binary text pattern (BIN Text Pattern), or hexadecimal text pattern (HEX Text Pattern) format. Refer to Section 5.2.6.9 "Compatibility with test pattern files of existing models" for file compatibility.
	Save	Saves a setting file in the binary pattern (Binary Pattern), binary text pattern (BIN Text Pattern), or hexadecimal text pattern (HEX Text Pattern) format. ***Note:*** The settings will not be read from the saved file if the file name is changed.
	Screen Copy	Prints a screen image. When configuring the print settings, select "Screen Copy" → "Setup" from the File menu on the MX180000A menu bar.
Edit	Undo	Restores the previous state.
	Cut	Over write: Cuts the pattern selected in the Pattern View area and transfers it onto the clipboard. The area that has been cut out becomes 0. Insert: Cuts the selected pattern with its address domain. After cutting, zero pattern with the same amount of the cut domain is added instead at the end of pattern length.
	Copy	Copies the pattern selected in the Pattern View area into the internal memory.

Table 5.2.6.1-1 Menu bar configuration (Cont'd)

Menu	Menu item	Description
Edit (continued)	Paste	Pastes the pattern copied in the internal memory to the cursor position.
	Jump	Moves the cursor to a specified address or pattern.
	Head	Moves the cursor to the start of the editing pattern.
	Tail	Moves the cursor to the end of the editing pattern.
	Marker	Moves the cursor to a position specified by the marker when set to ON.
	Address	Opens the **Input Address** dialog box. The cursor can be moved to the specified address position.
	Pattern	Opens the **Input Pattern** dialog box. Specifies a pattern string to search by binary digits, and a pattern to be masked by an "x". If a pattern matching the search condition is found in the editing pattern, the cursor moves to that position. Both forward search and backward search are supported. The search pattern can be specified in the **Input Pattern** dialog box. [Set ALL] Set all the bits to "1". [Reset ALL] Set all the bits to "0". [ALL X] Set all the bits to "Don't care" Select the search direction by clicking **Forward** or **Backward**, and then click [OK].
	Forward Next	Searches for a pattern that matches the search pattern set in the **Input Pattern** dialog box in the forward direction. If a matching pattern is found, the cursor moves to that position.
	Backward Next	Searches for a pattern that matches the search pattern set in the **Input Pattern** dialog box in the backward direction. If a matching pattern is found, the cursor moves to that position.
	Line	Specifies the number of characters per line in the Pattern View area. This is available when the pattern setting item Display is set to "Table".

[2] Pattern setting items

Table 5.2.6.1-2 Pattern setting items

<table>
<tr><th>Setting item</th><th>Description</th></tr>
<tr><td>Display</td><td>Select the display format in the Patter View area from “Time” or “Table”.
Time: The Pattern View area is displayed based on the time axis.
Table: The Pattern View area is displayed in a tabular format.</td></tr>
<tr><td>Format</td><td>Specify the pattern display format in the Pattern View area.
Available format depends on the Display setting.
<table>
<tr><td>Setting of Display</td><td>Option of Format</td></tr>
<tr><td>Time</td><td>Wave: The pattern is displayed by a waveform.
Bin: The pattern is displayed by a bit string.</td></tr>
<tr><td>Table</td><td>Bin: Binary
Hex: Hexadecimal</td></tr>
</table></td></tr>
<tr><td>Marker</td><td>Click this button to place a marker in the Pattern View area.
This is available when “Time” is selected for Display.</td></tr>
<tr><td>Focus</td><td>This is available when Marker is set to ON.
Select whether to activate a marker or cursor in the Pattern View area.</td></tr>
<tr><td>Edit Mode</td><td>Specify the pattern editing method from “Overwrite” or “Insert”. This must be specified in advance when executing Paste from the Edit menu or when performing direct editing in the Pattern View area (except for the Fill setting area).
Overwrite: The selected pattern is overwritten.
Insert: The editing pattern is inserted into the position of the selected pattern. Note that Data Length is not changed when Insert is selected. The inserted pattern therefore exceeds the Data Length value, and becomes invalid.</td></tr>
<tr><td>Range</td><td>Specify the pattern editing range from “Whole”, “Any”, or “Direct”.
Whole: All editing patterns are selected as the editing range.
Any: The Input Range dialog box (see Figure 5.2.6.1-2) is displayed when this button is clicked. The editing range can be specified by an address.
Direct: Select an arbitrary area by specifying addresses. Use the cursor to specify addresses.
Refer to Section 5.2.6.7 “Editing area” for details.</td></tr>
</table>

Table 5.2.6.1-2 Pattern setting items (Cont'd)

Setting item	Description
Fill	Edits the pattern part highlighted by the cursor. 0: The highlighted part in the Pattern View area is set to "0". 1: The highlighted part in the Pattern View area is set to "1". Reverse: The highlighted part in the Pattern View area is logically inverted. Pattern: The **Input Pattern** dialog box (see Figure 5.2.6.1-3) is displayed. The highlighted part in the Pattern View area can be edited in this dialog box. Repeat: The edited pattern for which the highlighted address is set to the first is repeated for the number of times specified here. Length: Specify the number of edit bits from the start address of the highlighted part. Set All: Sets all the bits selected by Length to "1". Reset All: Sets all the bits selected by Length to "0".
Zoom 	The waveform displayed in the Pattern View area can be enlarged or reduced by changing Zoom. The selectable scale is 1/8, 1/4, 1/2, 1, 2, 4, and 8. These buttons are available only when "Time" is set for Display and "Wave" is set for Format.

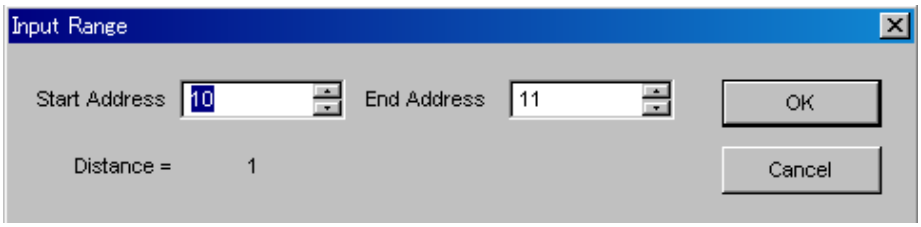


Figure 5.2.6.1-2 Input Range dialog box

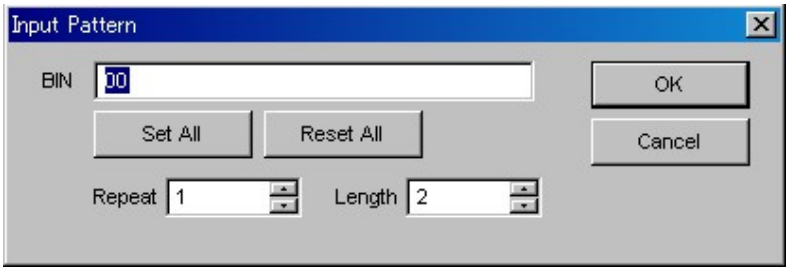


Figure 5.2.6.1-3 Input Pattern dialog box

[3] Pattern View area

The edited pattern is displayed in this area.
Double-clicking a pattern enables the bit value to be changed. Note that the pattern cannot be edited by a mouse operation when Display is set to Table and Format is set to Hex.

5.2.6.2 Editing Data pattern

When [Edit] is clicked while Data is selected for the test pattern, the **Pattern Editor** dialog box shown in Figure 5.2.6.2-1 is displayed.

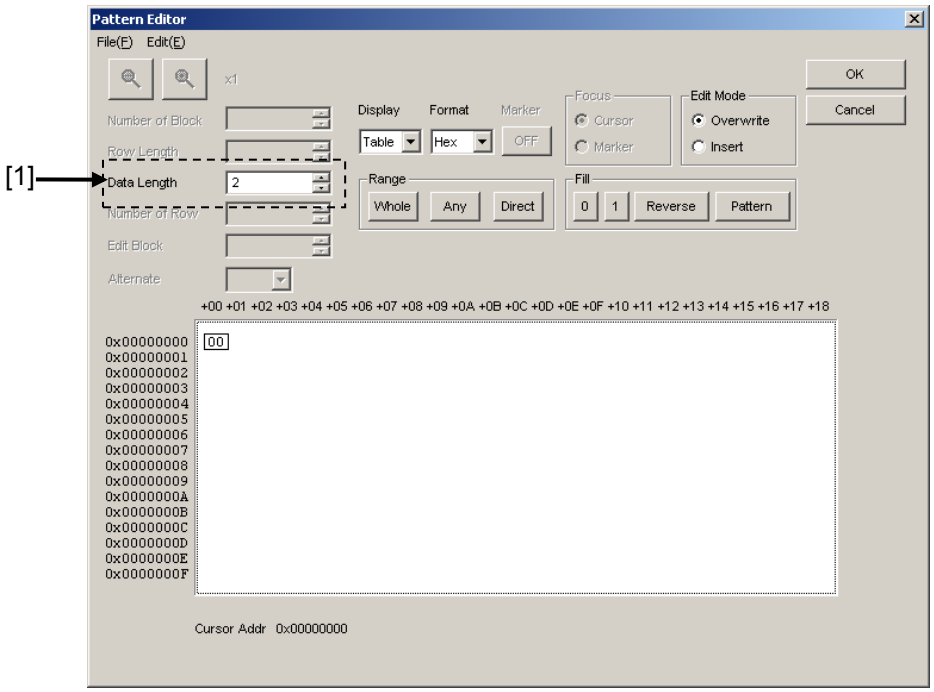


Figure 5.2.6.2-1 Pattern Editor dialog box for Data pattern

[1] Pattern setting item

Table 5.2.6.2-1 Pattern setting items (when Data is selected)

Setting item	Description
Data Length	Set the length of the Data pattern. The setting unit is one bit. 2 to 268,435,456 bits can be set, in 1-bit steps. In the case of 2ch Combination, 4 to 536,870,912 bits can be set, in 2-bit steps. In the case of 4ch Combination, 8 to 1,073,741,824 bits can be set, in 4-bit steps.

5.2.6.3 Editing Mixed pattern

When [Edit] is clicked while Mixed is selected for the test pattern, the **Pattern Editor** dialog box shown in Figure 5.2.6.3-1 is displayed.

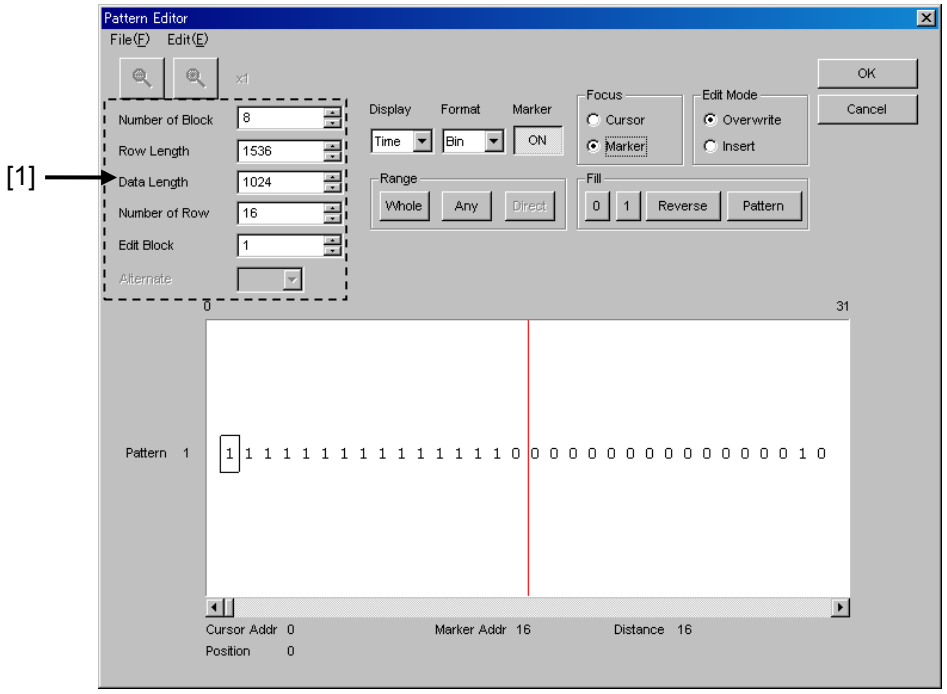


Figure 5.2.6.3-1 Pattern Editor dialog box for Mixed pattern

[1] Pattern setting items

Table 5.2.6.3-1 Pattern setting items (when Mixed is selected)

Setting item	Description
Number of Block	Set the number of blocks from 1 to 511, in 1-block steps.
Row Length	Set the row length. Can be set from 1,536 to 2,415,919,104 bits, in 256-bit steps. In the case of 2ch Combination, set from 3,072 to 4,831,838,208 bits in 512-bit steps. In the case of 4ch Combination, set from 6,144 to 9,663,676,416 bits in 1024-bit steps.
Data Length	Set the pattern length. Can be set from 1,024 to 268,435,456 bits, in 1-bit steps. In the case of 2ch Combination, set from 2,048 to 536,870,912 bits in 2-bit steps. In the case of 4ch Combination, set from 4,096 to 1,073,741,824 bits in 4-bit steps.
Number of Row	Set the number of rows from 1 to 16, in 1-row steps.
Edit Block	Specify the number of blocks to be edited.

Note:

The number of blocks and the number of rows are restricted as follows.

Number of blocks
1 to the smallest number among a to d, below, in 1-block steps
a) 511
b) INT (256 Mbit× x/ (Number of rows × Data Length'))
where Data Length' is:
●When Data Length is indivisible by (256 × x)
=(INT(Data Length/ (256 × x)) +1) × 256 × x
●When Data Length is divisible by (256 × x)
=Data Length
Maximum Block number should satisfy:
Data Length' x Number of Rows ×Number of Blocks ≤ 256 Mbits
c) INT ((256 Mbits +2^{31}) × x/(Row Length × Number of rows))
where x is:
1 for Independent
2 for 2ch Combination
4 for 4ch Combination
d) (Row Length – Data Length) × Number of blocks
≥2^31(2147483648)

Number of Rows
1 to the smallest number among a to c, below, in 1-row steps
a) 16
b) INT (256 Mbit × x/Data Length')
where Data Length' is:
●When Data Length is indivisible by (256 × x)
=(INT(Data Length/ (256 × x))+1) × 256 × x
●When Data Length is divisible by (256 × x)
=Data Length
Maximum Row number which meets:
Data Length' x Number of Rows x Number of Blocks ≤ 256 Mbits
c) INT ((256 Mbits +2^{31}) × x/Row Length)
where x is;
1 for Independent
2 for 2ch Combination
4 for 4ch Combination

5.2.6.4 Creating and editing test pattern

This section describes how to create and edit a test pattern in the **Pattern Editor** dialog box.

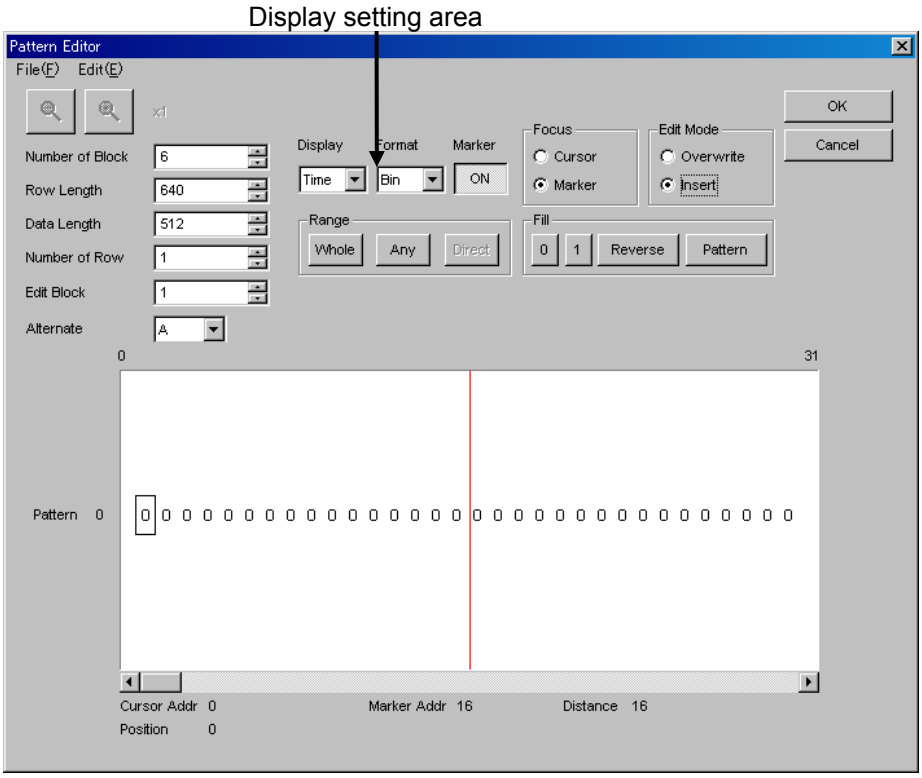


Figure 5.2.6.4-1 Display drop-down list

1. Select the Pattern View area display format from the Display drop-down list.

Table 5.2.6.4-1 Selection in Display setting area

Setting item	Description
Time	The test pattern is displayed and edited in a line with the horizontal time axis. The test pattern is displayed and can be edited with a waveform image or in binary.
Table	The test pattern is displayed and edited with a memory dump image. The test pattern is displayed and can be edited in binary or hexadecimal format.

2. For how to edit a test pattern in the **Pattern Editor** dialog box, refer to the corresponding section according to the display mode, as follows:

   When Time is selected: Refer to Section 5.2.6.5 “Editing in Time display mode”.

   When Table is selected: Refer to Section 5.2.6.6 “Editing in Table display mode”.

5.2.6.5 Editing in Time display mode

How to create and edit a test pattern in the Time display mode is described below.

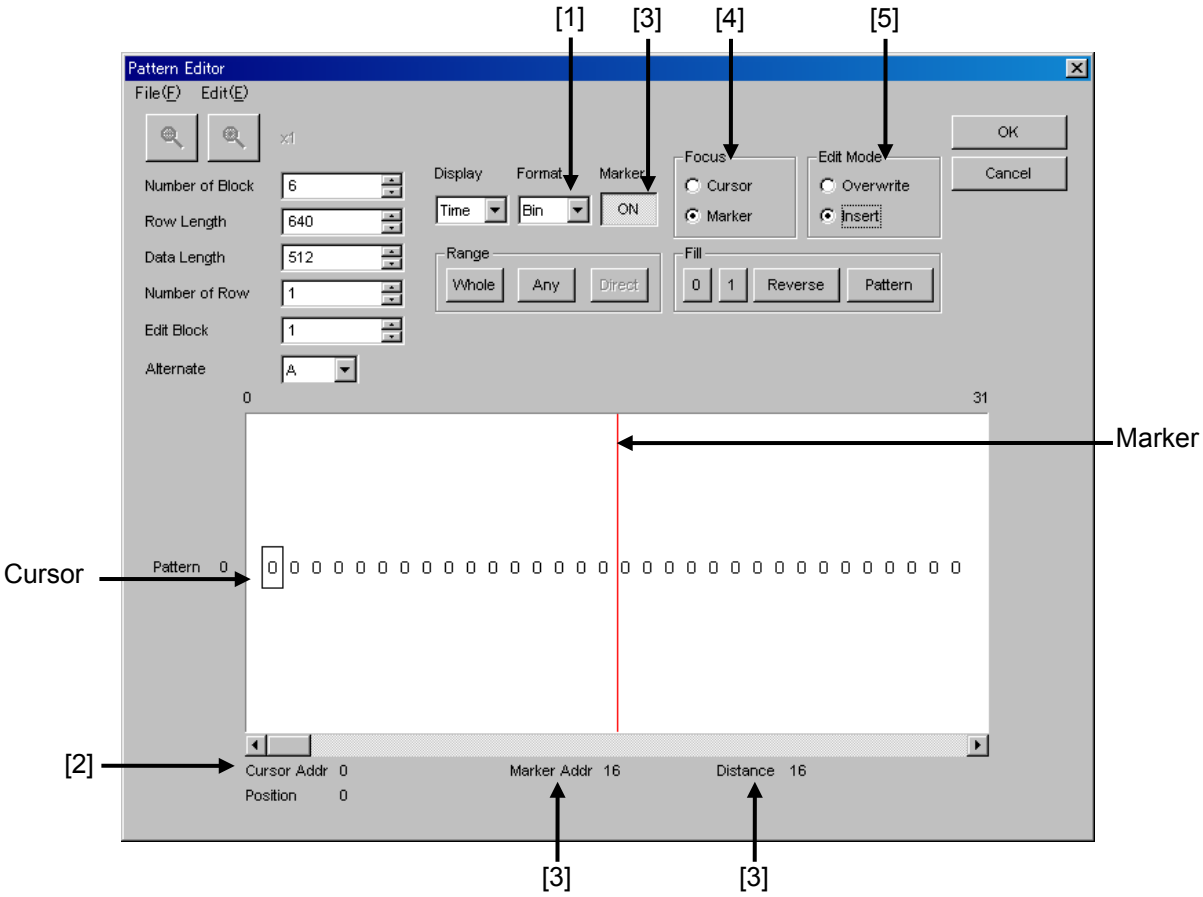


Figure 5.2.6.5-1 Editing in Time display mode

[1] Select the display format from the Format drop-down list in the **Pattern Editor** dialog box.

Table 5.2.6.5-1 Display format setting

Setting item	Description
Wave	A test pattern is displayed and edited with a waveform image. The waveform image can be enlarged and reduced using the Zoom In and Zoom Out buttons.
Bin	A test pattern is displayed and edited in binary.

[2] The address of the cursor is displayed.

[3] Set marker display ON/OFF.
The marker is displayed when the [Marker] is clicked and displayed as “ON”. The marker is not displayed when the button is clicked and displayed as “OFF”. The address of the marker and the distance between the cursor and marker are displayed in “Marker Addr” and “Distance”, respectively.

[4] Select the operation target.
The cursor is operated when **Cursor** is clicked, and the marker is operated when **Marker** is clicked.

[5] Set the editing mode.
Editing is performed in the insertion mode when **Insert** is clicked, and is performed in the overwriting mode when **Overwrite** is clicked.

5.2.6.6 Editing in Table display mode

How to create and edit a test pattern in the Table display mode is described below.

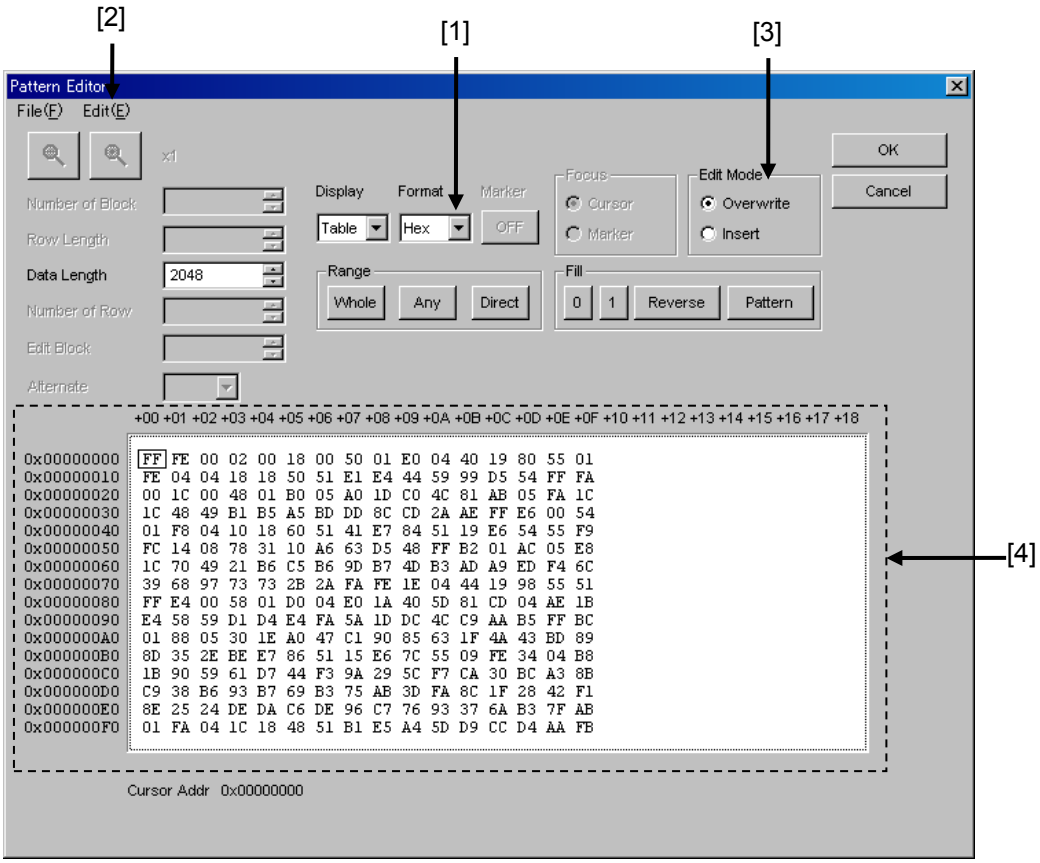


Figure 5.2.6.6-1 Editing in Table display mode

[1] Select the display format from the Format drop-down list in the **Pattern Editor** dialog box.

Table 5.2.6.6-1 Display format setting

Setting item	Description
Bin	A test pattern is displayed and edited in binary.
Hex	A test pattern is displayed and edited in hexadecimal format.

[2] The amount of data to be displayed in one line can be changed. Select "Line" from the Edit menu to open the **Line** dialog box. Enter the number of bytes per line in the textbox, and then click [OK].

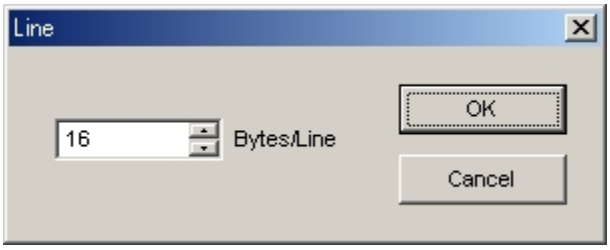


Figure 5.2.6.6-2 Line dialog box

[3] Set the editing mode.
Editing is performed in the insertion mode when **Insert** is clicked, and is performed in the overwriting mode when **Overwrite** is clicked.

[4] Use the 0 and 1 keys for pattern input when the display format is binary. Use 0 to 9 and A to F keys when the display format is hexadecimal.

5.2.6.7 Editing area

In the **Pattern Editor** dialog box, batch editing is possible for an area by selecting it consisting of multiple bits. In this area, perform replace input using the Fill group box, or use Cut, Copy, and Paste editing commands. The selection area setting procedure by using buttons in the Range group box is described below.

The function of each button is as follows:

Table 5.2.6.7-1 Area specification buttons

Button	Function
Whole	Specifies entire of the pattern as the selection area.
Any	Sets an arbitrary area as the selection area by specifying addresses. The address is specified by entering values in the **Input Range** dialog box.
Direct	Sets an arbitrary area as the selection area by specifying addresses. The address is specified by using a cursor.

How to specify the selection area using the [Any] is as follows.

Figure 5.2.6.7-1 Input Range dialog box

1. Enter the start address of the selection area in the Start Address spin box.
2. Enter the end address of the selection area in the End Address spin box.
3. Click [OK] to set the specified area as the selection area. The selection area is highlighted in the **Pattern Editor** dialog box.

How to specify the selection area using the [Direct] is as follows.

1. Click [Direct].
   The [Direct] is depressed and the Direct mode is entered. Note that pattern input and editing cannot be performed in the Direct mode.
2. Specify the start position of the selection area by double-clicking the desired position or by moving the cursor to that position and pressing the [Enter] key.
3. Specify the end position of the selection area. Display the desired position for the selection area by selecting “Jump” from the Edit menu, and then double-click the position or move the cursor to that position and press the [Enter] key.
4. The selection area is now completely set.

The selection area can also be specified by the following step.

1. Drag the mouse to select an area.

5.2.6.8 Inputting pattern

How to input a pattern by using the buttons in the Fill group box is described below. The function of each button is as follows:

Table 5.2.6.8-1 Fill button functions

Button	Function
0	Replaces the bit of the cursor position or the bits in the selection area to "0".
1	Replaces the bit of the cursor position or the bits in the selection area to "1".
Reverse	Inverts the bit of the cursor position or the bits in the selection area.
Pattern	Inputs an arbitrary pattern repeatedly.

- How to input a pattern using the [Pattern] is as follows.

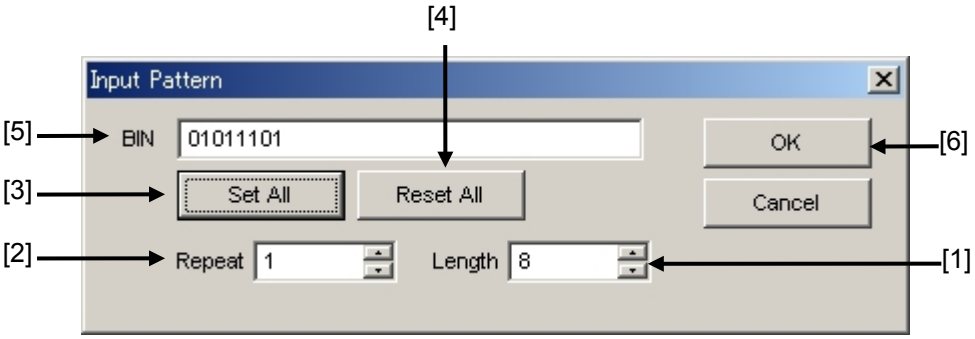


Figure 5.2.6.8-1 Input Pattern dialog box

[1] Enter the number of bits to be input.

[2] Enter the number of specified pattern repetition times.

[3] Click [Set ALL] to set all the bits to "1".

[4] Click [Reset ALL] to set all the bits to "0".

[5] Input a pattern into the BIN or HEX textbox.

[6] Click [OK] to input the pattern to the cursor position.

Note:

When the **Input Pattern** dialog box is displayed while the selection area is specified, a repetition of the specified pattern is applied to the selection area, regardless of the number of repetition times specified in the Repeat spin box.

5.2.6.9 Compatibility with test pattern files of existing models

Pattern files (.PTN) created for the following existing models can be loaded into the **Pattern Editor** dialog box of the MU183020A.

MP1632C	Digital Data Analyzer
MP1761A/B/C	Pulse Pattern Generator
MP1762A/C/D	Error Detector
MP1775A	Pulse Pattern Generator
MP1776A	Error Detector
MU181020A/B	Pulse Pattern Generator
MU181040A/B	Error Detector

5.3 Adding Errors

An error can be added to output data by configuring the error occurrence settings on the **Error Addition** tab.

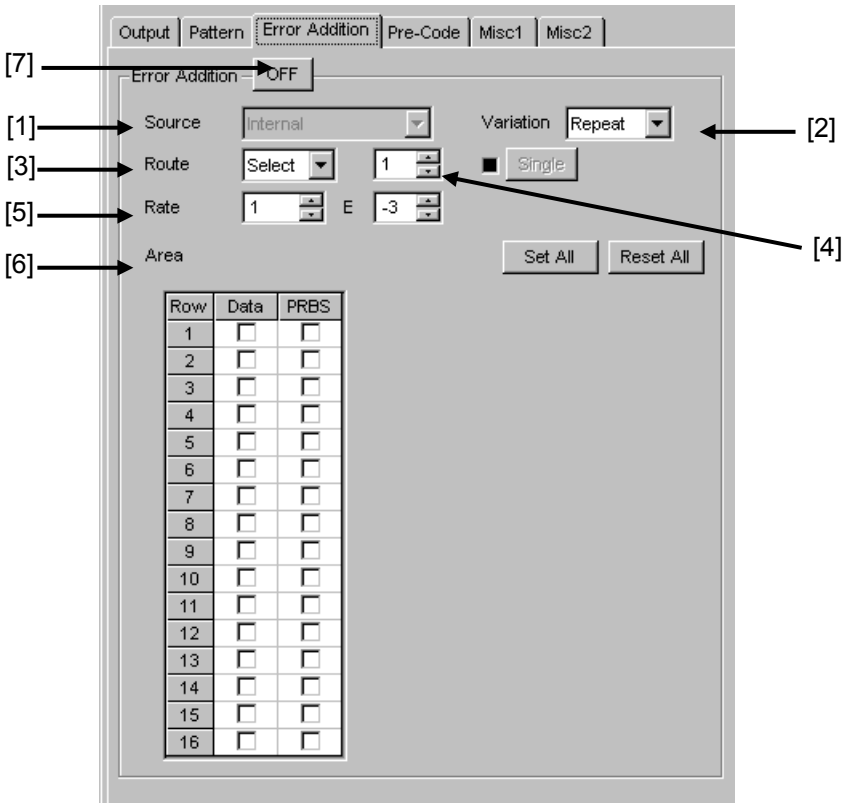


Figure 5.3-1 Error Addition tab

[1] Selecting error adding source

Select the method for generating the timing to add a specified bit error to the test pattern.

Table 5.3-1 Error addition source setting

Selection item	Description
Internal	The error addition timing is generated by the internal circuit.
External-Trigger	The error addition timing is generated in synchronization with the trigger edge of the external signal input from the Auxiliary Input connector. This cannot be set when Error-Injection is not set for AUX Input on the **Misc1** tab.
External-Disable	The error addition timing is generated by the internal circuit, but an error is not added when the external signal input from the Auxiliary Input connector is low. This cannot be set when Error-Injection is not set for AUX Input on the **Misc1** tab.

[2] When “Internal” or “External-Disable” is selected, select the error addition variation. Select the error insertion method when adding an error (internal Gating).

Table 5.3-2 Error insertion method setting

Selection item	Description
Repeat	An error is continuously inserted.
Single	An error is inserted once when the button is clicked. In Combination function, errors as many as the number of Combined channels are inserted once when the button is clicked. Note that the following restrictions apply. Available only when “Internal” or “External-Disable” is selected from the Source drop-down list.

[3] Select the method for inserting an error addition route.

Table 5.3-3 Error addition route setting

Selection item	Description
Scan	A route for which a 1/1 signal is demultiplexed by 32 is changed each time an error is inserted.
Select	An error is inserted to the specified route.

[4] Specify a route to generate a 1-bit error for the test pattern. The route can be specified from 1 to 32, in single steps.

Note that the following restrictions apply.

(a) This setting is valid even when the error addition function is set to OFF.

(b) This setting is invalid when Scan is selected in the Route drop-down list.

[5] Select the bit error rate to generate a 1-bit error for the test pattern.

xE–n: x can be set to 1 to 9, in single steps.
n can be set to 3 to 12, in single steps.

Note that the following restrictions apply.

(a) The setting is valid even when the error addition function is set to OFF.

(b) This setting is invalid when the error addition variation setting is set to Single.

(c) This setting is invalid when the error addition source is set to External-Trigger.

(d) x can be set to 1 to 5 when n is set to 3.

(e) Maximum insertion bit rate is 5E–3.

[6] For the Mixed pattern, select the block (Data/PRBS and Block No.) where a bit error is to be inserted.

[7] Enables/disables generating a bit error for the test pattern.

ON: Enables the error addition function.
OFF: Disables the error addition function.

Note that this setting affects all error addition functions. When set to OFF, bit error addition triggered by an external error signal is also disabled.

5.4 Setting Pre-Code Function

Pre-Code function can be set when Combination in 5.6.2 “Multi-channel Function” is selected for the MU183020A-x22, MU183020A-x23 or MU183021A.

Since this function supports DQPSK, and DPQPSK technologies, it can calculate and output Data as shown in the following Pre-Code logic diagram.

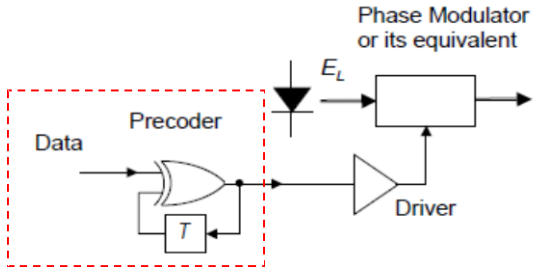


Figure 5.4-1 Pre-Code Logic (DQPSK) Diagram

To set the Pre-Code function, click the **Pre-Code** tab.

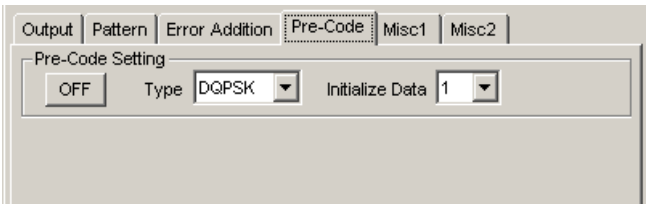


Figure 5.4-2 Pre-Code tab

Note:

Pre-Code Settings are common to all channels where Combination function is set.

5.4.1 Pre-Code setting

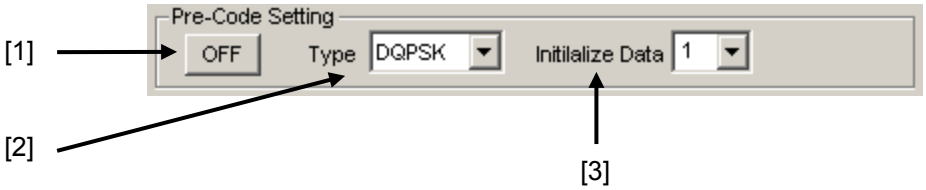


Figure 5.4.1-1 Pre-Code Setting Area

Table 5.4.1-1 Pre-Code Setting item

No.	Item	Function
[1]	Pre-Code ON/OFF	Sets Pre-Code ON and OFF
[2]	Type	Sets Pre-Code modulation method When 2ch Combination selected: DQPSK When 2ch Combination CH Sync selected: DPQPSK
[3]	Initialize Data	Sets Pre-Code to default values (Default: 1)

5.5 Misc1 Function

The settings of the signal generating method, synchronized output, and auxiliary input/output can be configured.
Click the **Misc1** tab of the MU183020A operation window to configure the Misc function.

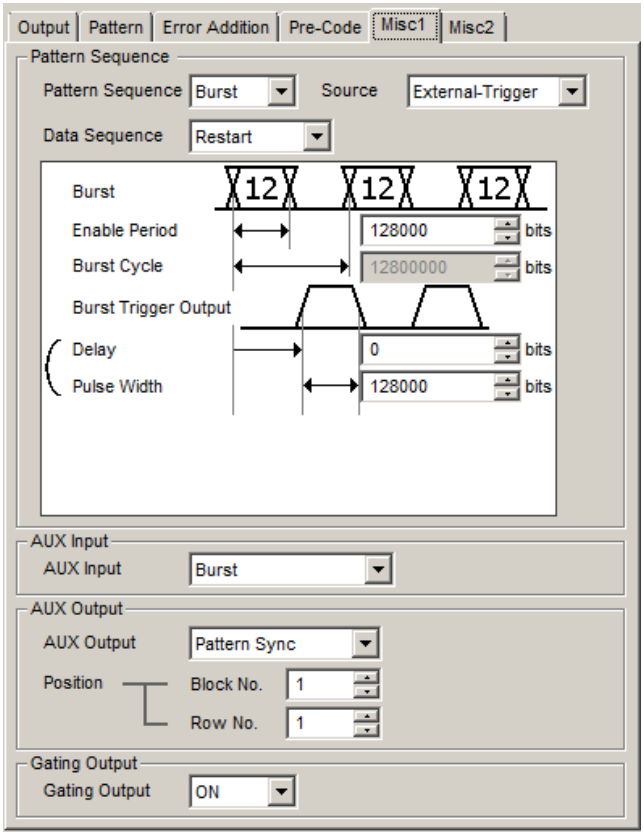


Figure 5.5-1 Misc1 tab

Table 5.5-1 Setting items

Setting area	Description
Pattern Sequence	Set the test pattern generating method.
AUX Input	Configure the settings for the auxiliary input function.
AUX Output	Configure the settings for the auxiliary output function.
Gating Output	Set the timing signal output.

Settings on the **Misc1** tab are common to Data 1 to Data 4.
Settings related to the pattern length depend on the Data1 settings.

5.5.1 Setting pattern sequence

Select the signal generating method.

Figure 5.5.1-1 Selecting pattern sequence

Table 5.5.1-1 Pattern sequence setting

Selection item	Description
Repeat	Select when transmitting the test pattern Repeat data. Mainly used for electric device evaluation.
Burst	Select when transmitting the test pattern Burst data. Mainly used for long-distance optical transmission tests such as an optical circulating loop test, and packet communications evaluation. The target test patterns are PRBS, Zero-Substitution, Data, and Mixed (Data).

5.5.1.1 Setting Repeat pattern

Select “Repeat” from the Pattern Sequence drop-down list to transmit the test pattern Repeat data.

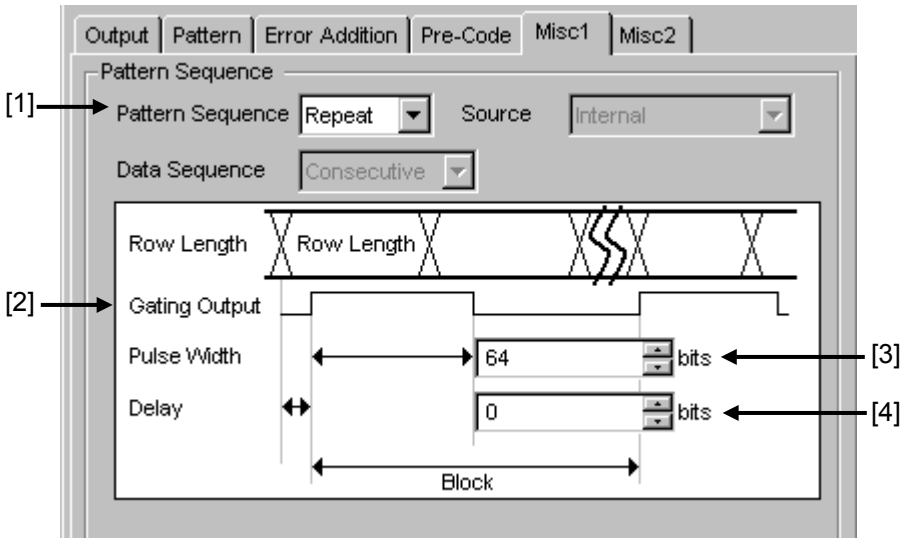


Figure 5.5.1.1-1 Setting items for Repeat pattern sequence

[1] Select “Repeat” from the Pattern Sequence drop-down list, and generate continuous test patterns and data signals.

[2] Configure the settings related to the synchronization signal that is output from the Gating Output connector.
The period of data signal synchronization output is calculated from the following expression, according to the signal type.

Table 5.5.1.1-1 Gating output setting range

Periodic Signal	Setting Range
PRBS, Data, Zero-Substitution	Least common multiple of Pattern length' and 128 * In the case of 2ch Combination: Least common multiple of Pattern Length and 256 In the case of 4ch Combination: Least common multiple of Pattern Length and 512
Mixed	(Row length × Number of Rows × Block count)

*: Pattern Length' is the value obtained by multiplying the Pattern Length setting until it becomes 512*N or more if it is 128*N or less.
N=Number of Combination channels

[3] In the Pulse Width textbox, specify the high level pulse width of the synchronization signal that is output from the Gating Output connector. The pulse width should be a multiple of 8. The Data Length setting value is calculated from the following expression, according to the signal type.

Table 5.5.1.1-2 Pulse width setting range

Periodic Signal	Setting Range
PRBS, Data, Zero-Substitution	0 to (Least common multiple of Pattern length and 128) – 128 (The maximum settable number is 34,359,738,240) Setting step: 8 bit In the case of 2ch Combination (the target test patterns are PRBS, Data, and Zero-Substitution) is 0 to (Least common multiple of Pattern Length and 256) – 256 and the setting step becomes 16 bits. (The maximum settable number is 68,719,476,480) In the case of 4ch Combination (the target test patterns are PRBS, Data, and Zero-Substitution) is 0 to (Least common multiple of Pattern Length and 512) –512 and the setting step becomes 32 bits. (The maximum settable number is 137,438,952,960)
Mixed	0 to (Row length × Number of Rows × Block count) – 128 (The maximum settable number is 2,415,918,976) Setting step: 8 bit In the case of 2ch Combination is 0 to (Row length × Number of rows × Block count) – 256, and the setting step becomes 16 bits. In the case of 4ch Combination is 0 to (Row length × Number of rows × Block count) –512, and the setting step becomes 32 bits.

*: When the pattern length is 511 bits or less, specify the pattern length as an integer multiple so that it becomes 512 bits or more.

At 2ch Combination, when the pattern length is 1023 bits or less, specify the length as an integer multiple so that it becomes 1024 bits or more.

At 4ch Combination, when the pattern length is 2047 bits or less, specify the length as an integer multiple so that it becomes 2048 bits or more.

[4] In the Delay textbox, specify how many bits the data output is delayed from the beginning of the data pattern.
The delay should be a multiple of 8. The delay is calculated from the following expression, according to the signal type.

Table 5.5.1.1-3 Delay setting range

Periodic Signal	Setting Range
PRBS, Data, Zero-Substitution	0 to (Least common multiple of Pattern length and 128) – 128 (The maximum settable number is 34,359,738,240) Setting step: 8 bit In the case of 2ch Combination (the target test patterns are PRBS, Data, and Zero-Substitution), is 0 to (Least common multiple of Pattern Length and 256) –256 and the setting step becomes 16 bits. (The maximum settable number is 68,719,476,480) In the case of 4ch Combination (the target test patterns are PRBS, Data, and Zero-Substitution), is 0 to (Least common multiple of Pattern Length and 512) –512 and the setting step becomes 32 bits. (The maximum settable number is 137,438,952,960)
Mixed	0 to (Row length × Number of Rows × Block count) –128 (The maximum settable number is 2,415,918,976) Setting step: 8 bit In the case of 2ch Combination is 0 to (Row length × Number of rows × Block count) –256, and the setting step becomes 16 bits. In the case of 4ch Combination is 0 to (Row length × Number of rows × Block count) –512, and the setting step becomes 32 bits.

*: When the pattern length is 511 bits or less, specify the pattern length as an integer multiple so that it becomes 512 bits or more.

At 2ch Combination, when the pattern length is 1023 bits or less, specify the length as an integer multiple so that it becomes 1024 bits or more.
At 4ch Combination, when the pattern length is 2047 bits or less, specify the length as an integer multiple so that it becomes 2048 bits or more.

5.5.1.2 Setting Burst pattern

Select "Burst" from the Pattern Sequence drop-down list to transmit the test pattern Burst data.

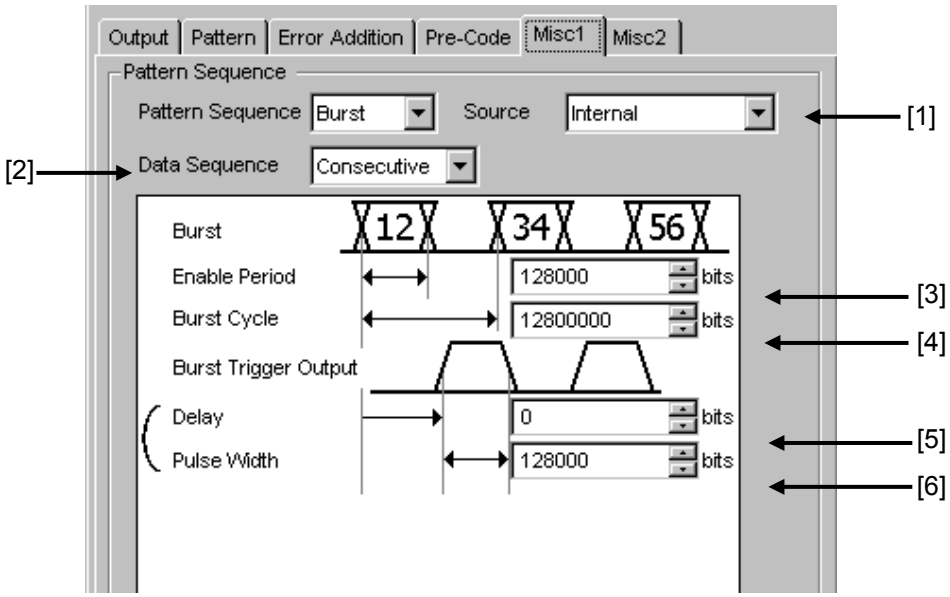


Figure 5.5.1.2-1 Setting items for Burst pattern sequence

Note:

The Burst Trigger Output signal is output from the Gating Output connector.

[1] Select the timing to generate test patterns with the Burst signal.

Table 5.5.1.2-1 Burst setting items

Selection item	Description
Internal	The Burst signal occurrence timing is generated by the internal circuit.
External-Trigger	The Burst signal occurrence period is generated based on the gate signal input from the external connector. Burst pattern generation starts at the rising edge of the input gate signal.
External-Enable	The Burst signal occurrence period is generated based on the gate signal input from the external connector. The Burst data is generated when the gate signal is high, and is not generated when the gate signal is low.

[2] Specify the burst pattern generating sequence.

Table 5.5.1.2-2 Burst pattern generation sequence setting

Selection item	Description
Restart	The specified test pattern is restarted from the beginning each time a Burst data signal occurs.
Consecutive	The specified test pattern is continuously output between Burst data signals.
Continuous	The specified test pattern is continuously output, and outputs other than the Burst occurrence timing are masked.

[3] When External-Trigger or Internal is selected from the Source drop-down list ([1] in Figure 5.5.1.2-1), set the continuous signal generation period for the Burst cycle of the test pattern to be input to the AUX Input connector, by entering the number of bits in the **Enabled Period** box.

The setting ranges for Enable Period are shown in Table 5.5.1.2-3.

[4] When Internal is selected from the Source drop-down list ([1] in Figure 5.5.1.2-1), set the Burst cycle (one cycle of the Burst signal of the test pattern to be input) by entering the number of bits in the **Burst Cycle b**ox.

The setting ranges for Burst Cycle are shown in the following table.

Table 5.5.1.2-3 Setting ranges for Enable Periods and Burst Cycles

No. of Channel Combinations	Enable Period (bit)	Burst Cycle (bit)	Setting Steps (bit)
1	When Internal is set: 12 800 to 2 147 483 392	25 600 to 2 147 483 648	256
	When External-Trigger is set: 12 800 to 2 147 483 648		
2	When Internal is set: 25 600 to 4 294 966 784	51 200 to 4 294 966 296	512
	When External-Trigger is set: 25 600 to 4 294 967 296		
4	When Internal is set: 51 200 to 8 589 933 568	102 400 to 8 589 934 592	1024
	When External-Trigger is set: 51 200 to 8 589 934 592		

Note:

A Disable period of at least 512 bits is required between Burst Cycle and Enable Period.
The Disable period is doubled at 2ch Combination and quadrupled at 4ch Combination.

[5], [6] Set the Burst timing signal that is output from the Burst Trigger Output connector.

Delay: Specify how many bits the data output is delayed from the beginning of the Burst data pattern.

Pulse Width: Specify the high level pulse width of the synchronization signal that is output from the Burst Trigger Output connector.

The setting ranges for Delay and Pulse Width are shown in the following table.

Table 5.5.1.2-4 Setting ranges for Delay and Pulse Width

No. of Channel Combinations	Delay (bit)	Pulse Width (bit)	Setting Steps (bits)
1	0 to (Burst cycle–128)	0 to (Burst cycle–128)	8
2	0 to (Burst cycle–256)	0 to (Burst cycle–256)	16
4	0 to (Burst cycle–512)	0 to (Burst cycle–512)	32

5.5.2 Setting AUX Input

Use the Aux Input connector when inserting an error based on the externally-generated timing signal.
The following table shows the functions that use Aux Input connector.

Figure 5.5.2-1 Setting item for AUX Input

Table 5.5.2-1 Setting items

Selection item	Description
Error Injection	Select when inserting an error based on the timing of an external signal. This is used when “External-Trigger” or “External-Disable” is selected from the Source drop-down list on the **Error Addition** tab (refer to Section 5.3 “Adding Errors” for details).
Burst	Select when Burst is selected from the Pattern Sequence drop-down list, and External-Trigger or External Enable is selected from the Source drop-down list. Refer to Section 5.5.1.2 “Setting Burst pattern” for details.

5.5.3 Setting AUX Output

The output settings of auxiliary signals, such as the synchronization signal, can be configured.

5.5.3.1 Setting 1/N Clock

When "1/N Clock" is selected from the AUX Output drop-down list, a clock can be output from the AUX Output connector in synchronization with the test pattern.

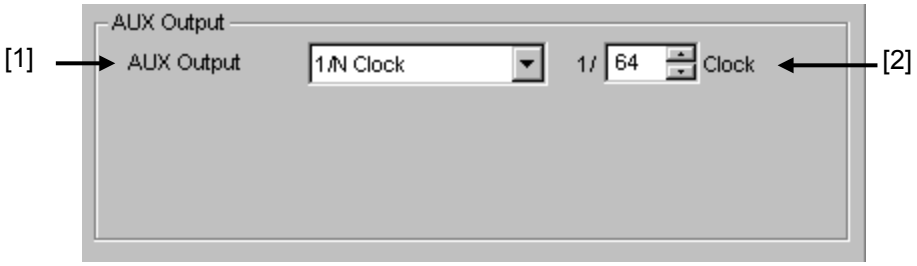


Figure 5.5.3.1-1 Setting items for AUX Output Clock

[1] When "1/N Clock" is selected from the AUX Output drop-down list, a clock can be output from the AUX Output connector in synchronization with the test pattern.

[2] The frequency dividing ratio for the synchronization clock can be set.
The setting range for the setting frequency is 4 to 512, stepping 2.

5.5.3.2 Setting Pattern Sync

A timing signal can be generated in synchronization with the test pattern period.

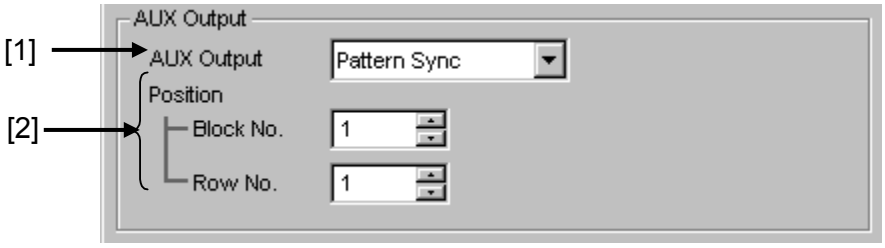


Figure 5.5.3.2-1 Setting items for AUX Output Pattern Sync

[1] When "Pattern Sync" is selected from the AUX Output drop-down list, a pulse signal can be output from the AUX Output connector in synchronization with the set data pattern period.

[2] The synchronization signal pulse generation position can be set.
The setting method varies depending on the test pattern.

Table 5.5.3.2-1 Synchronization signal pulse generation position setting

Test pattern	Description
PRBS, Data, Zero-Substitution	A signal pulse is generated in a pattern period. The pulse position can be specified within the range below, starting from the beginning of the pattern. 1 to {(Least common multiple of Pattern Length* and 128)–135}, in 8-bit steps. The maximum settable number is 34,359,738,105 In the case of 2ch Combination: 1 to {(Least common multiple of Pattern Length* and 256) –287}, in 16-bit steps. The maximum settable number is 68,719,476,209 In the case of 4ch Combination: 1 to {(Least common multiple of Pattern Length* and 512)–543}, in 32-bit steps. The maximum settable number is 137,438,952,417
Mixed (Data)	A signal pulse is generated during the entire block generation pattern period. The pulse position can be specified by the positions of Block and Row.

*: When the pattern length is 511 bits or less, specify the Pattern length as an integer multiple so that it becomes 512 bits or more.

At 2ch Combination, when the pattern length is 1023 bits or less, specify the length as an integer multiple so that it becomes 1024 bits or more.

At 4ch Combination, when the pattern length is 2047 bits or less, specify the length as an integer multiple so that it becomes 2048 bits or more.

5.5.3.3 Setting Burst Output2

When Burst is selected from the Pattern Sequence drop-down list, a timing signal similar to the Burst Trigger Output signal can be outputted from the AUX Output connector.

Table 5.5.3.3-1 Burst Output2 setting

Setting item	Description
Delay	Specify how many bits the data output is delayed from the beginning of the Burst data pattern. The setting range is similar to Table 5.5.1.2-4 Setting ranges for Delay and Pulse Width.
Pulse Width	Specify the high level pulse width of the synchronization signal that is output from the Burst Trigger Output connector. The setting range is similar to Table 5.5.1.2-4 Setting ranges for Delay and Pulse Width.

5.5.3.4 Setting output to Off

When set to OFF, the AUX Output connector does not output signals.

5.5.4 Setting Gating Output

Set the output from the Gating Output connector to On or Off.

Figure 5.5.4-1 Gating Output Setting

Table 5.5.4-1 Gating Output Setting

Selection item	Description
ON	The Gating Output connector outputs synchronization signals set by pattern sequence.
OFF	The Gating Output connector does not output signals.

5.6 Misc2 Function

On the **Misc 2** tab, you can perform the Clock Setting and Combination Setting of multiple channels.

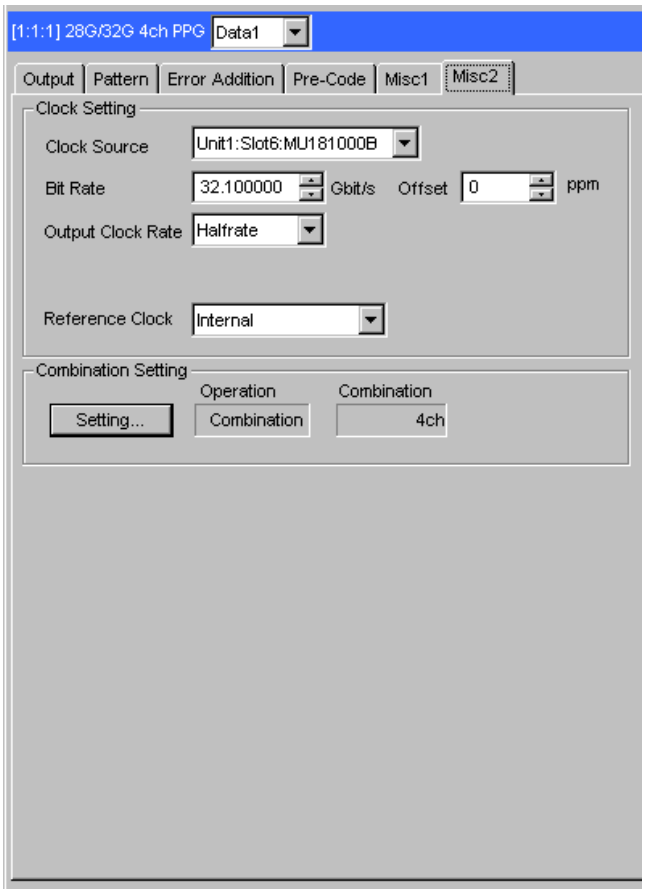


Figure 5.6-1 Misc2 tab

5.6.1 Setting Clock

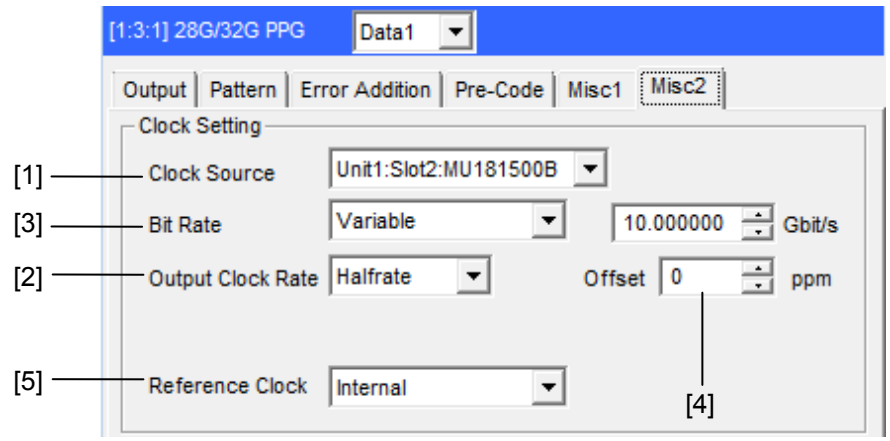


Figure 5.6.1-1 Setting items for Clock setting (when MU181500B is selected)

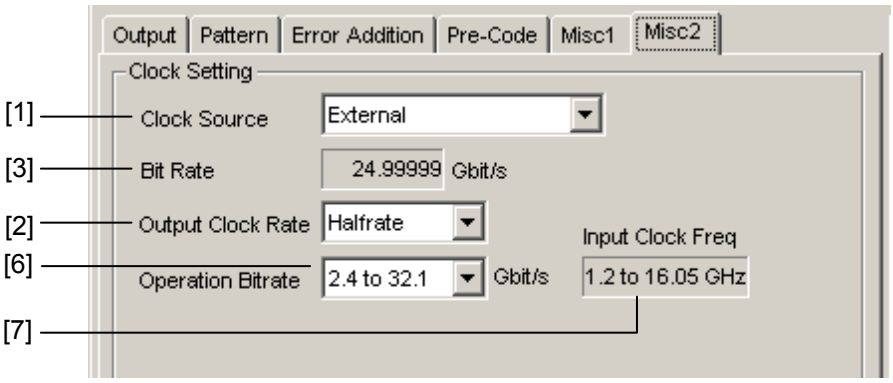


Figure 5.6.1-2 Setting items for Clock setting (when External is selected)

[1] Clock source can be selected from the drop-down list

Table 5.6.1-1 Clock Source setting items

Selection item	Description
External	The clock input into Ext Clock Input connector of MU183020A or MU183021A.
MU181000A	The clock of a synthesizer module that is installed in MP1800A or MT1810A.
MU181000B	
MU181500B	The clock of a jitter module that is installed in MP1800A or MT1810A.

[2] Set the output bit rate.
Full Rate Clock: Clock frequency is same as output data rate.
Half Rate Clock: Clock frequency is half of output data rate.

When Clock Source is MU181000A/B or MU181500B

[3] Set the output bit rate. Select [Variable] or a preset standard value. For details, refer to 5.1.4 “Setting bit rate”.

[4] Set the frequency offset of the synthesizer module within the range from –1000 to 1000.

Offset is not displayed when Clock source is [External].

[5] Set the reference clock of MU181000A/B.

When Clock Source is External

[3] Bit rate of output data is displayed.

[6] Output clock frequency range of MU183020A or MU183021A is displayed.

[7] Frequency of clock input to Input connector of MU183020A is displayed.

If “MU181500B” is selected in the Clock Source drop-down list [1], the frequency of the clock input to the MU181500B is displayed. The relationship between operation bitrate and input clock frequency that vary depending on the options selected in the list boxes [2] and [6] is shown below. The values enclosed in parentheses apply when the 32G bit/s Extension Option (MU183020A/MU183021A-x01) is not installed.

Table 5.6.1-2 Relationship Between Operation Bitrate and Input Clock Frequency (When Using External Clock)

Output Clock Rate setting	Operation Bitrate setting (Range)	Input Clock Freq value (Display)	Relationship Between Bitrate and Clock Frequency
Full Rate Clock	2.4 to 16.0 Gbit/s	2.4 to 16.0 GHz	Operate at 1/1 clock
	16.0 to 20.4 Gbit/s	8.0 to 10.2 GHz	Operate at 1/2 clock
	20.0 to 32.1 (28.1) Gbit/s	10.0 to 16.05 (14.05) GHz	Operate at 1/2 clock
	25.0 to 32.1 (28.1) Gbit/s	6.25 to 8.025 (7.025) GHz	Operate at 1/4 clock
Half Rate Clock	2.4 to 32.1 (28.1) Gbit/s	1.2 to 16.05 (14.05) GHz	Operate at 1/2 clock
	25.0 to 32.1 (28.1) Gbit/s	6.25 to 8.025 (7.025) GHz	Operate at 1/4 clock

Table 5.6.1-3 Relationship Between Operation Bitrate and Input Clock Frequency (When Using MU181500B and External Clock)

Output Clock Rate setting	Operation Bitrate setting (Range)	Input Clock Freq value (Display)	Relationship Between Bitrate and Clock Frequency
Full Rate Clock	2.4 to 15.0 Gbit/s	2.4 to 15.0 GHz	Operate at 1/1 clock
	12.5 to 20.0 Gbit/s	6.25 to 10.0 GHz	Operate at 1/2 clock
	20.0 to 30.0 (28.1) Gbit/s	10.0 to 16.05 (14.05) GHz	Operate at 1/2 clock
	25.0 to 32.1 Gbit/s	6.25 to 8.025 GHz	Operate at 1/4 clock
Half Rate Clock	2.4 to 30.0 (28.1) Gbit/s	1.2 to 15.0 (14.05) GHz	Operate at 1/2 clock
	30.0 to 32.1 Gbit/s	7.5 to 8.025 GHz	Operate at 1/4 clock

Clock connection and screen settings

Depending on the used clock source, change both clock connection with MU183020A and settings in the screen. The procedure for connecting MU183020A, clock source, and jitter source and setting the screen items that varies by used clock source is described below.

Note:

Install the MU181000A/B synthesizer and/or the MU181500B Jitter Modulation Source to the mainframe to which MU183020A is installed when the modules are included in the following configuration.

Connection and setting of MU183020A used by the following configurations are described.

(1) MU183020A, MU181000A/B synthesizer, and MU181500B Jitter Modulation Source

(2) MU183020A and MU181000A/B synthesizer

(3) MU183020A, MU181500B Jitter Modulation Source, and external clock source

(4) MU183020A and external clock source

Description is given according to the following configuration of MP1800A:

- MU181000B is installed to Slot1-2.
- MU183020A is installed to Slot3.
- MU181500B is installed to Slot5-6.

In addition, the procedure is described from the state that the clock source setting for each MU183020A/MU183021A and MU181500B is External (Default).

5.6.1.1 MU183020A, MU181000A/B synthesizer, and MU181500B Jitter Modulation Source

Connecting to the clock

For connecting the MU183020A, MU181000A/B, and MU181500B to the clock, refer to the connection diagram and description in 3.2.2 “Adding Jitter to Output Signal”.

Setting in the screen

1. Select “Unit1:Slot2: MU181000B” from the Synthesizer Clock Source drop-down list in the MU181500B screen to make MU181500B and MU181000B track each other. (Refer to Figure 5.6.1.1-1.)
2. Select “Unit1:Slot6: MU181500B” from the Clock Source drop-down list in the MU183020A screen to make MU183020A and MU181500B track each other. (Refer to Figure 5.6.1.1-2.)
3. Now, you can set the bit rate of the output data to the Bit Rate box in the MU183020A screen. Figure 5.6.1.1-2 shows an example when the output data is set to 32.1 Gbit/s.

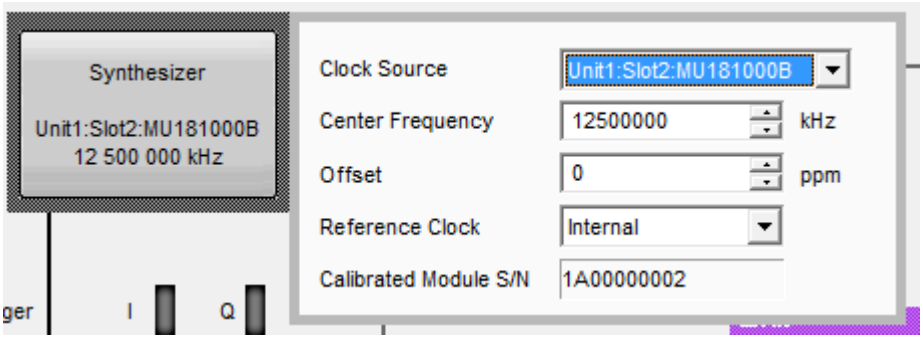


Figure 5.6.1.1-1 MU181500B Clock Source Settings

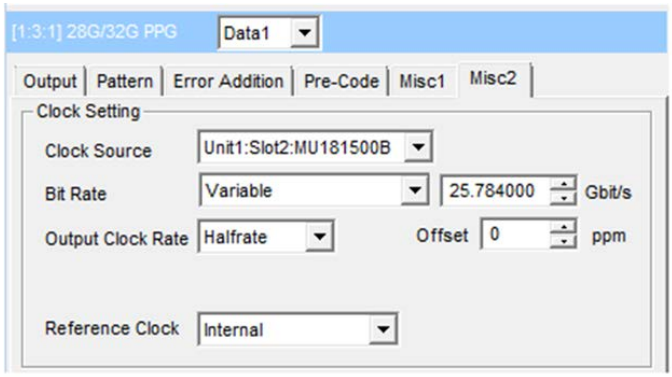


Figure 5.6.1.1-2 Clock Source Settings (When Tracking Operation of Jitter and Synthesizer)

Note:

Follow the above-mentioned procedure and set to make MU181500B and MU181000B track each other. If the steps are performed in the wrong order, a warning dialog box appears as shown in Figure 5.6.1.1-3.

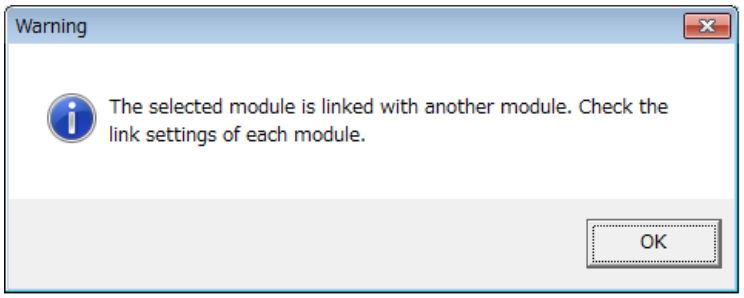


Figure 5.6.1.1-3 Warning Dialog Box for Module-Tracking Operation

5.6.1.2 MU183020A and MU181000A/B synthesizer

Connecting to the clock

For connecting the MU183020A and MU181000A/B to the clock, refer to the connection diagram and description in 3.2.1 “Connecting with MU183040A”.

Setting in the screen

1. Select “Unit1:Slot2: MU181000B” from the Clock Source drop-down list in the MU183020A screen to make MU183020A and MU181000B track each other.
2. Now, you can set the bit rate of the output data to the Bit Rate box in the MU183020A screen. Figure 5.6.1.2-1 shows an example when the output data is set to 12.5 Gbit/s.

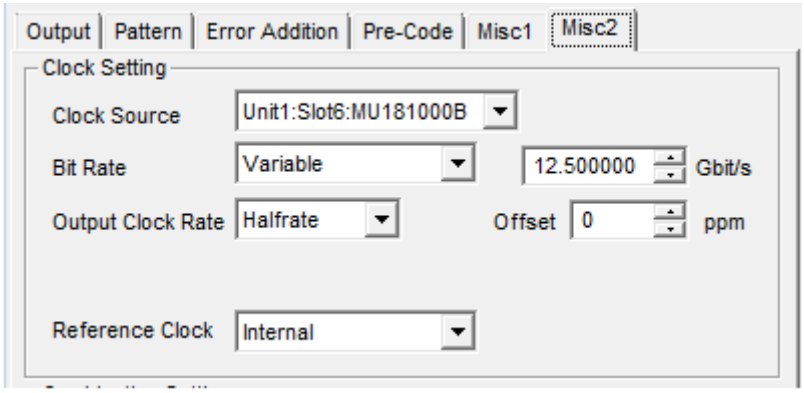


Figure 5.6.1.2-1 Clock Source Settings (When Tracking with Jitter)

5.6.1.3 MU183020A, MU181500B Jitter Modulation Source, and external clock source

Connecting to the clock

For connecting MU183020A and MU181500B to the external clock, refer to the connection diagram and description in 3.2.2 “Adding Jitter to Output Signal”, replacing MU181000A with “external clock source”.

Setting in the screen

1. Select “Unit1:Slot6: MU181500B” from the Clock Source drop-down list in the MU183020A screen to make MU183020A and MU181500B track each other.
2. In the MU183020A screen, select a bit rate of data to output from the Operation Bitrate drop-down list. To output 28 Gbit/s data, select “2.4 to 30 Gbit/s” as shown in the example of Figure 5.6.1.3-1.
3. To the Ext Clock Input connector of the MU181500B, input the clock of the frequency displayed in the Input Clock Freq box in the MU183020A screen. In the example in Figure 5.6.1.3-1, 14 GHz clock is input to output 28 Gbit/s data.
4. The Bit Rate box in the MU183020A screen displays the bit rate of the output data. Check that the clock that is input in step 3 can change the bit rate of the output data.

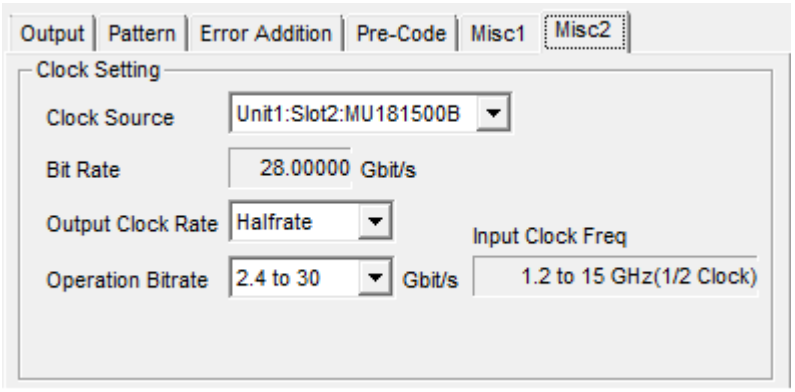


Figure 5.6.1.3-1 Clock Source Settings (When Using Jitter and External Clock Source)

5.6.1.4 MU183020A and external clock source

Connecting to the clock

For connecting MU183020A to the clock, refer to 3.2.3 “Using External Clock”.

Setting in the screen

1. In the MU183020A screen, select “External” from the Clock Source drop-down list.
2. In the MU183020A screen, select a bit rate band of data to output from the Operation Bitrate drop-down list. In the example in Figure 5.6.1.4-1, select “2.4 to 32.1 Gbit/s” to output 28 Gbit/s data.
3. To the Ext Clock Input connector of the MU183020A, input the clock of the frequency displayed in the Input Clock Freq box in the MU183020A screen. In the example in Figure 5.6.1.4-1, 14 GHz clock is input to output 28 Gbit/s data.
4. The Bit Rate box in the MU183020A screen displays the bit rate of the output data. Check that the clock that is input in step 3 can change the bit rate of the output data.

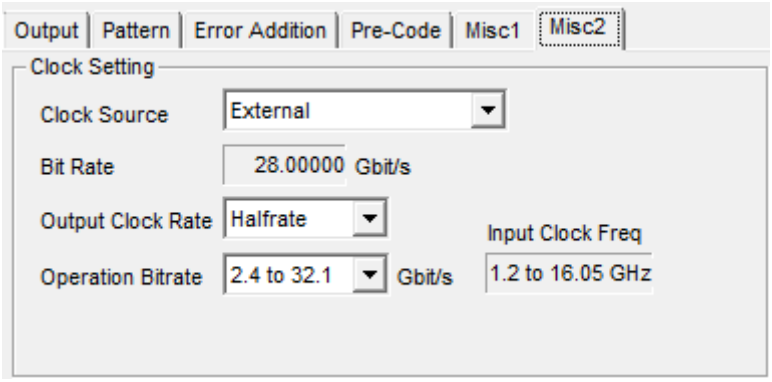


Figure 5.6.1.4-1 Clock Source Settings (When Using External Clock Source)

5.6.2 Multi-channel Function

MU183020A and MU183021A provide the Multi-channel functions that can generate data combining outputs from multiple channels.

The Multi-channel functions include the Combination and Channel Synchronization functions.

Available functions vary depending on model and its option.

Combination Function Types

(1) 4ch Combination: MU183021A

(2) 2ch Combination: MU183020A-x22, MU183020A-x23, MU183021A

Channel Synchronization Function Types

(1) CH Synchronization: MU183020A-x22, MU183020A-x23, MU183021A

(2) 2ch CH Synchronization: MU183021A

(3) Inter modules CH Synchronization: MU183020A, MU183021A

Table 5.6.2-1 Multi-channel functions that the respective models support

Model/Option	2ch Combi*	4ch Combi*	2ch CH Sync*	CH Sync*	Inter Module CH Sync*
MU183020A-x12 MU183020A-x13	–	–	–	–	–
MU183020A-x22 MU183020A-x23	✓	–	–	✓	✓
MU183021A	✓	✓	✓	✓	✓

*: MU183020A-x31 or MU183021A-x30 is required.

5.6.2.1 Combination Function

The Combination function can synchronize generation or reception of patterns among channels of MU183020A/MU183021A and MU183040A/MU183041A and evaluate 40 Gbit/s application and 100 Gbit/s application.

By combining four 28 Gbit/s channels by the MU183021A, the serial data at 111.8 Gbit/s of OTU4 (Optical channel Transport Unit 4) can be generated.

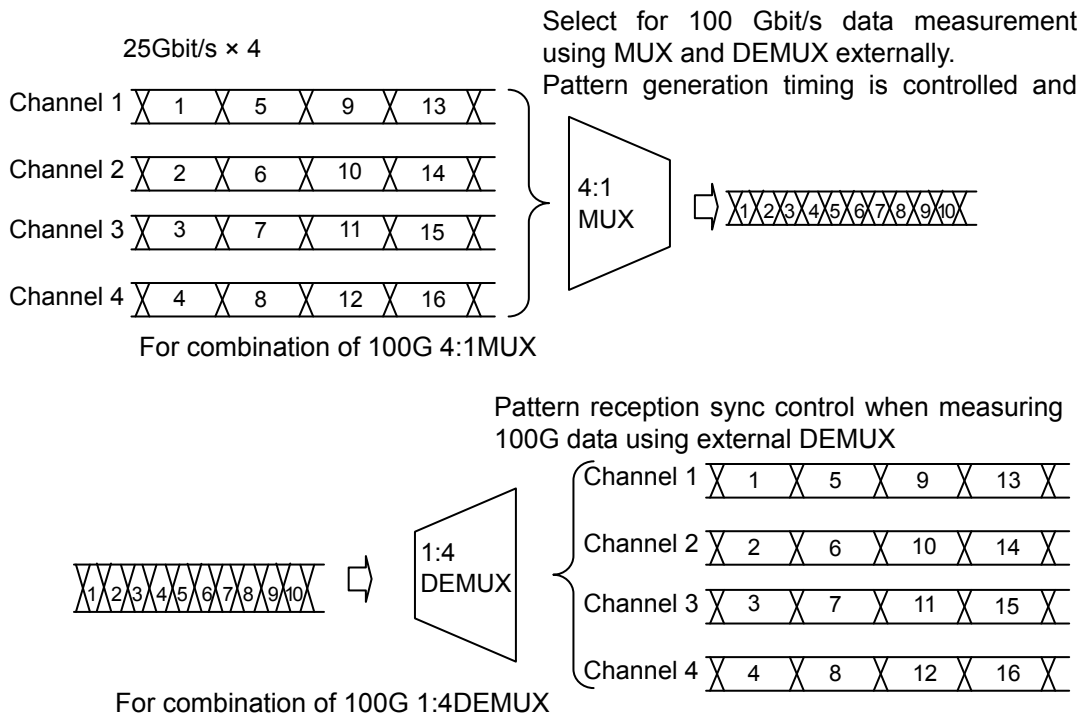


Figure 5.6.2.1-1 4ch Combination pattern generation/reception

By combining two channels of 20 Gbit/s data, 40 Gbit/s serial data that is bit rate of 40 GbE or OTU3 can be generated.

Different from the conventional method of combining four 10 Gbit/s data, this function can evaluate multiple DUTs by using a single MP1800A or MT1810A

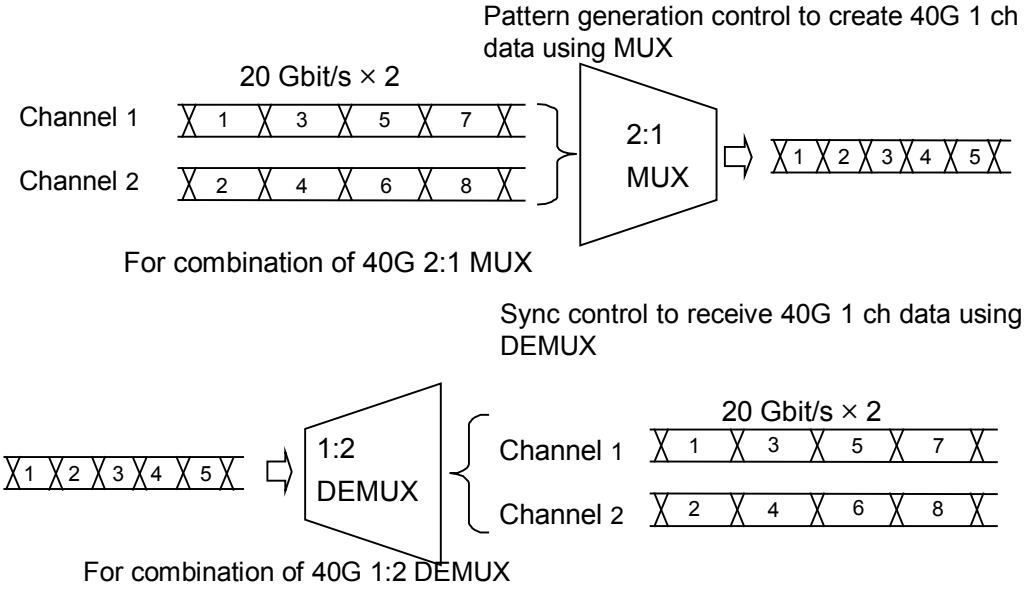


Figure 5.6.2.1-2 2ch Combination pattern generation/reception

5.6.2.2 Synchronization Function

Channel Synchronization function synchronizes the timing of data of multiple channels.
This function can also synchronize the timing of inter-modules (MU183020As and MU183021As). In addition, you can adjust the time delay between channels by setting the skew.

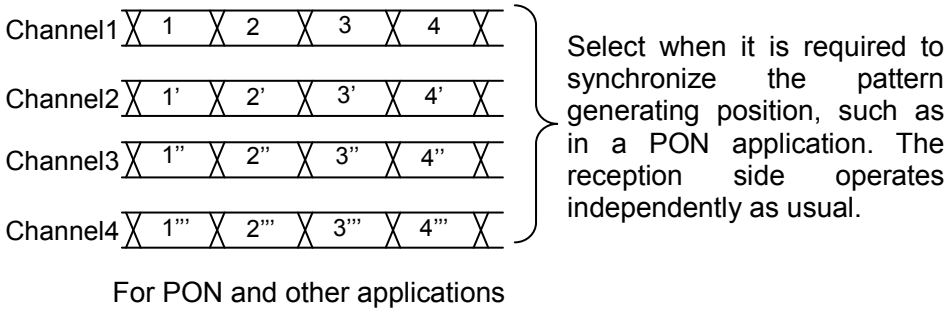


Figure 5.6.2.2-1 Channel Synchronization pattern generation/reception

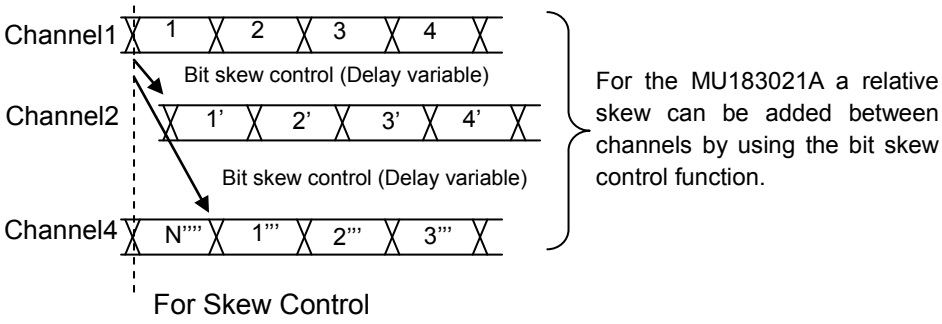


Figure 5.6.2.2-2 Skew Channel Synchronization Pattern

MU183021A can synchronize two signals Combination1-2 and Combination3-4 that are combined separately by 2ch Combination function.

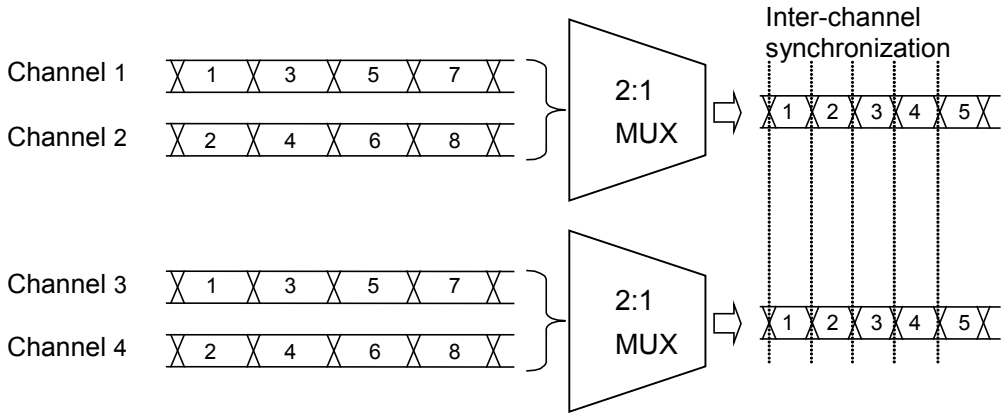


Figure 5.6.2.2-3 Channel Synchronization of 2Ch Combination

5.6.2.3 Combination Setting

To use the Multi-channel function, click [Setting...] on the **Misc2** tab, and then configure the function in the **Combination Setting** dialog box.

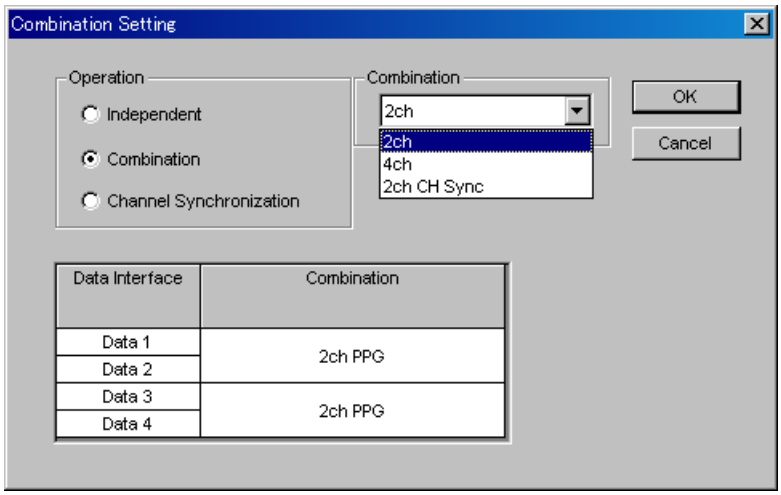


Figure 5.6.2.3-1 Combination Setting dialog box (2ch Combination)

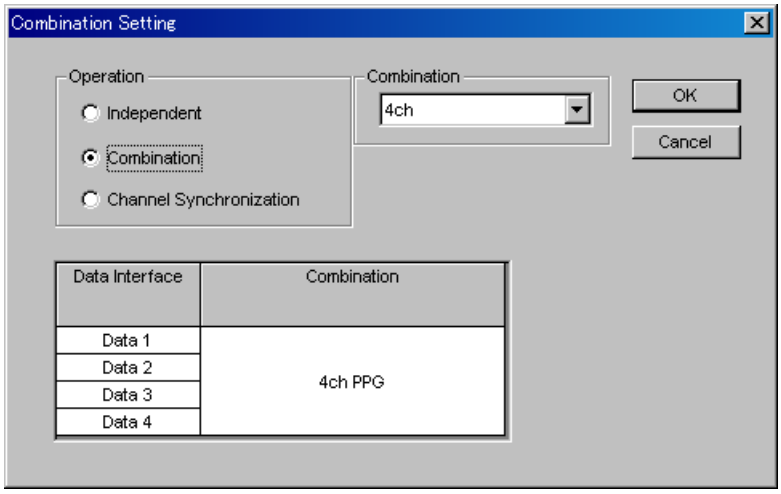


Figure 5.6.2.3-2 Combination Setting dialog box (4ch Combination)

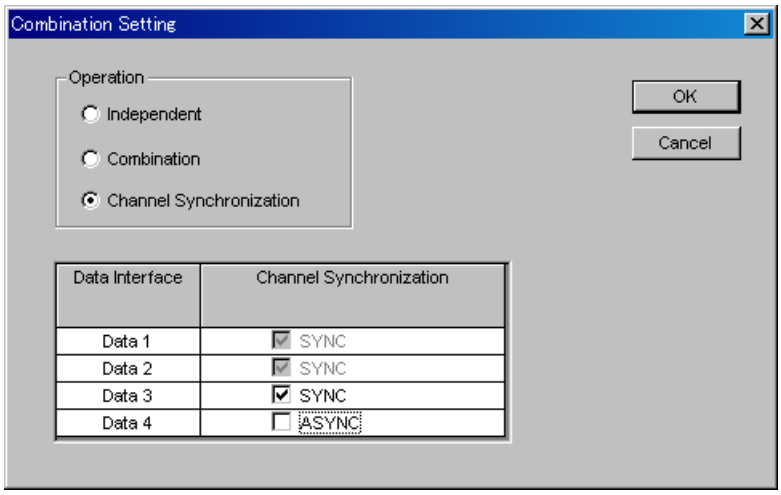


Figure 5.6.2.3-3 Combination Setting dialog box (Channel Synchronization)

Table 5.6.2.3-1 Setting items for Combination Setting

Operation Settings		Description
Independent		Selects when operating channel of MU183020A/MU183021A independently.
Combination	2ch*1,*2	Sets the Combination function for two channels.
	4ch*2	Sets the Combination function for four channels of MU183021A.
	2ch CH Sync*2	Sets the Combination function to two channels of MU183021A and sets the Channel Synchronization function to two combined signals.
Channel Synchronization*1, *2		Sets the Channel Synchronization function to all channels.

*1: MU183020A-x22, MU183020A-x23 and MU183020A-x31 are required.

*2: MU183021A-x30 is required.

5.6.3 Setting the Grouping function

The Grouping function allows you to group and share the settings on the Pattern and Output tabs between MU183020A and MU183021A channels. This function is useful when configuring multiple channels with the same settings.

Also, you can configure the settings in the Pattern and Output tabs of multiple MU183020As and MU183021As at a time.

Note:

Though the Grouping function allows you to configure the settings of the Output and Pattern tabs at a time, the period of time required until they are configured is the same as that required when separately configuring each of channels.

Procedure for setting the Channel Grouping function

[1] In the **Grouping Setting** area of the **Misc2** tab, click [Setup].

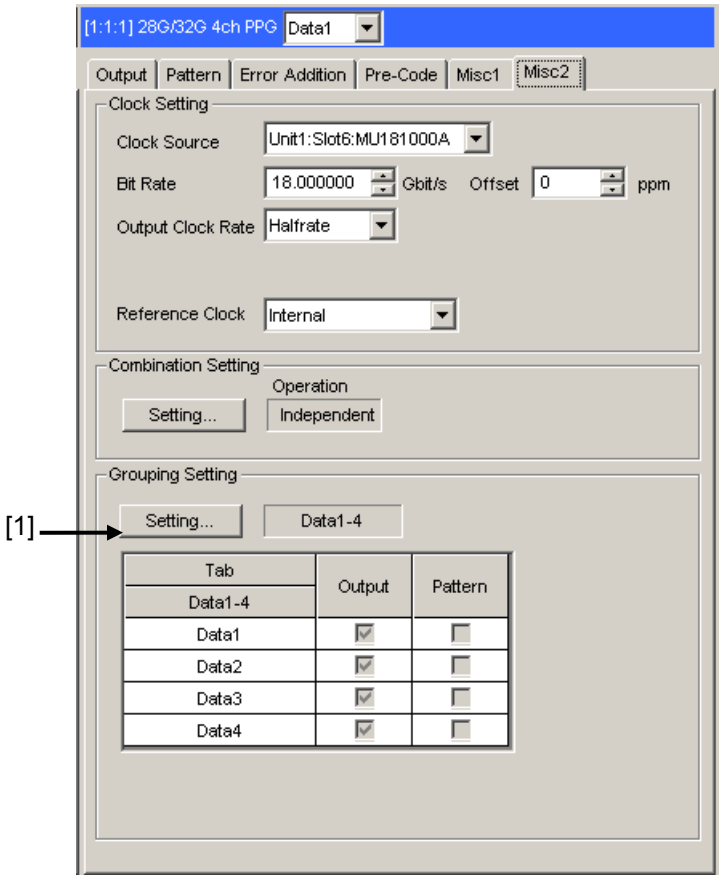


Figure 5.6.3-1 Grouping Setting

[2] In the **Grouping Setting** dialog box, select the check boxes of Tabs (Output and Pattern) and Data Interfaces that you want to group together.
Clicking [Set All] selects all the check boxes, and clicking [Reset All] clears all the check boxes. For MU183021A, you can select one of the following settings:

- Setting that groups Data1 to Data4 together
- Setting that groups Data1 and Data2, and Data3 and Data4 together, respectively

For details on tabs and setting items to be grouped together, refer to Table 5.6.3-1.

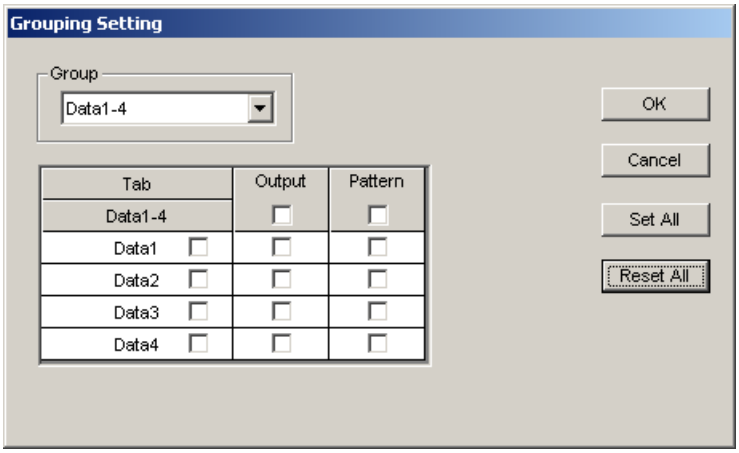


Figure 5.6.3-2 Grouping Setting Dialog Box (When Data1-4 is Selected)

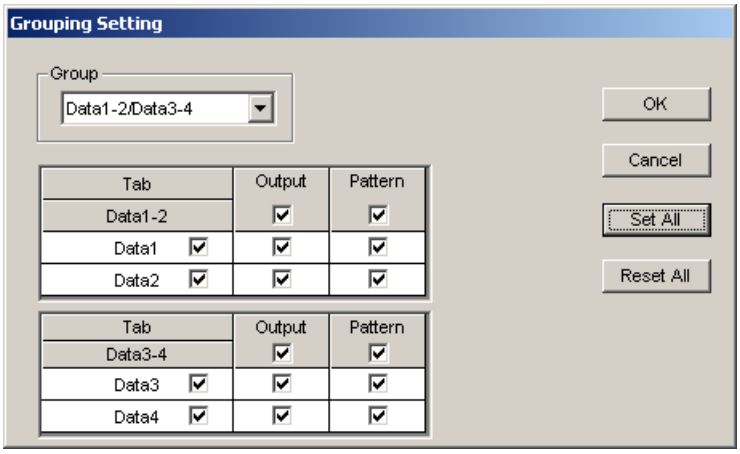


Figure 5.6.3-3 Grouping Setting Dialog Box (When Data1-2/Data3-4 is Selected)

Notes:

- When interworking to the MP1825B 4Tap Emphasis, the **Output Tab** check boxes cannot be selected.
- When the Output tabs are grouped together, it is impossible to interwork to the MP1825B 4Tap Emphasis.
- The Module Grouping function is available when at least two check boxes of each tab are selected.

[3] Click [OK] to close the **Grouping Setting** dialog box. Then, the DataInterface settings of the Master are shared by the Data Interfaces that are grouped together. (Master: Data Interface with the lowest Data Interface number among Data Interfaces selected at [2]) Then, the grouped tabs operate using the same settings.
When the grouping function is enabled, a color bar appears at the upper part of the tab.

Data1-2 (or Data1-4): Blue (Master Data1)
Data3-4: Purple (Master Data3)

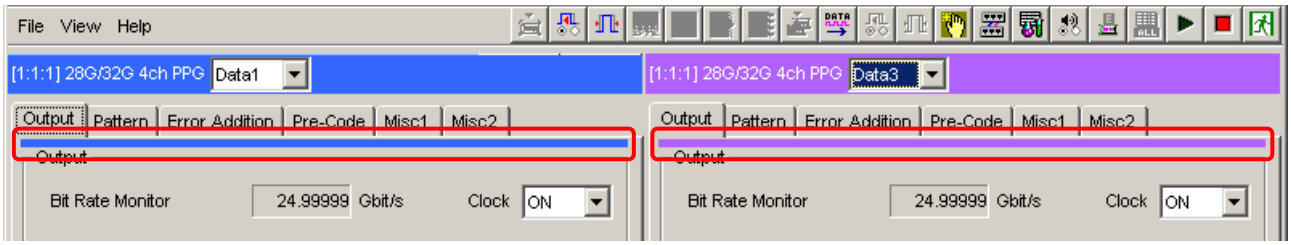


Figure 5.6.3-4 Indication That Appears When the Grouping Function is Enabled

Table 5.6.3-1 Grouping Objects

Tab	Main Category	Sub-Category		Whether Supported or Not
Pattern	Test Pattern	Pattern Selection		Yes
	PRBS	Length		Yes
		Logic		Yes
		Mark Ratio		Yes
		Edit		Yes
	Zero-substitution	Logic		Yes
		Length		Yes
		Zero-Substitution Length		Yes
		Addition Bit		Yes
		Edit		Yes
	Data	Logic		Yes
		Length		No
		Edit		No
	Mixed Data	Logic		Yes
		Number of Blocks (Display)		No
		Row Length (Display)		No
		Data Length (Display)		No
		Number of Rows (Display)		No
		Edit		No
		PRBS	Pattern	No
			Mark Ratio	Yes
		Scramble		No
		Scramble Setup		No
		PRBS Sequence		No

Table 5.6.3-1 Grouping Objects (Cont'd)

Tab	Main Category	Sub-Category	Individual Setting Item	Whether Supported or Not
Output	Data/XData Output ON/OFF			Yes
	Clock Output ON/OFF			Yes
	Amplitude/Offset			Yes
	Data/XData Selection	Tracking		Yes
		Level Guard		Yes
		Level Guard Setup	Maximum Amplitude	Yes
			Offset limit	Yes
		Defined Interface		Yes
			Amplitude	Yes
			Offset switching	Yes
			Offset	Yes
			External ATT Factor	Yes
		Cross Point		Yes
		Half Period Jitter		Yes
		Delay		No
			Calibration	Yes
		Jitter Input		Yes

Procedure for setting the Module Grouping function

[1] Click the **File** menu, click [Module Grouping], and then click [Setup].

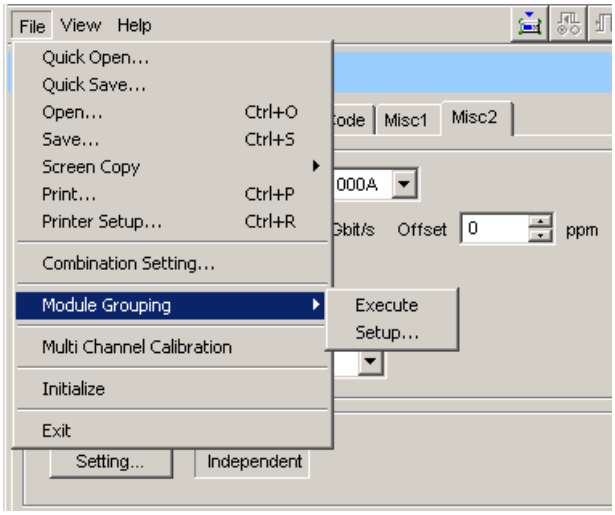


Figure 5.6.3-5 Module Grouping Menu

[2] In the **Grouping Setting** dialog box, select the check boxes of Tabs (Output and Pattern) and Slot Nos. that you want to group together. The module with the lowest Slot No. is assumed to be the master module.
Clicking [Set All] selects all the check boxes, and clicking [Reset All] clears all the check boxes. For details on tabs and setting items to be grouped together, refer to Table 5.6.3-1.

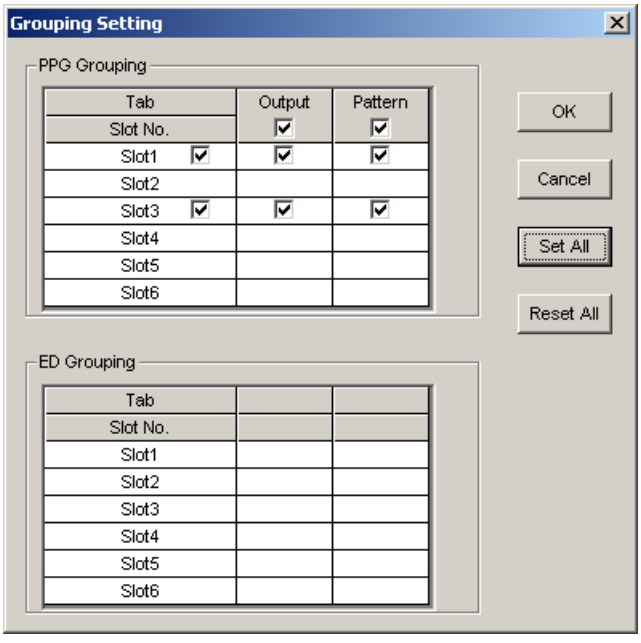


Figure 5.6.3-6 Grouping Setting Dialog Box

Notes:

- The Module Grouping function is available when the model name and option(s) of the modules match each other.
- When interworking to the MP1825B 4Tap Emphasis, the **Output Tab** check boxes cannot be selected.
- When the Output tabs are grouped together, it is impossible to interwork to the MP1825B 4Tap Emphasis.
- The Module Grouping function is available when at least two check boxes of each tab are selected.

[3] Click [OK] to close the **Grouping Setting** dialog box.

[4] Click the Module Grouping function button, and the settings items of the master module will be shared by the modules you want to group together.

Figure 5.6.3-7 Module Grouping Function Button

5.7 Inter-module Synchronization Function

To use the Inter-module synchronization function, press the Combination Setting module function button and set the parameters on the Combination Setting screen.
Inter-module synchronization function synchronizes the timing of modules using two sets of MU183020A or MU183021A. Refer to the release notes for the installation slots in the modules.

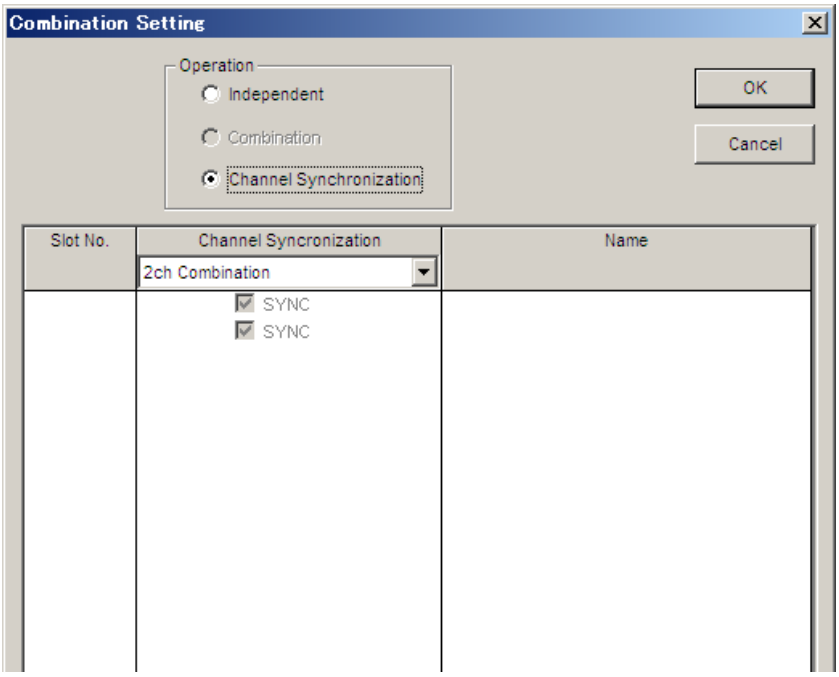


Figure 5.7-1 Combination Setting dialog box

Table 5.7-1 Setting items for Combination Setting

Operation Settings		Description
Independent		Select when operating the MU183020A or MU183021A independently.
Channel Synchronization	CH Sync*1, *2	Sets the Channel Synchronization function to all channels of the target modules.
	2ch Combination *1, *2	Sets the 2ch Combination to the target modules and sets the Channel Synchronization between modules.
	4ch Combination*2	Sets the 4ch Combination to the target modules and sets the Channel Synchronization among modules.

*1: MU183020A-x22, MU183020A-x23 and MU183020A-x31 are required.

*2: MU183021A-x30 is required.

5.8 Multi Channel Calibration Function

Calibration must be executed to use the Multi Channel function or the Inter-module Synchronization function under the optimum conditions. These functions are required when changing the configuration such as rearranging the modules installed in the main frame (MP1800A or MT1810A).

When calibration is required, a message dialog box (Figure 5.8-1) is displayed when selecting the Channel Synchronization, Combination, or Inter-module Synchronization setting. To execute Combination, click [Yes].

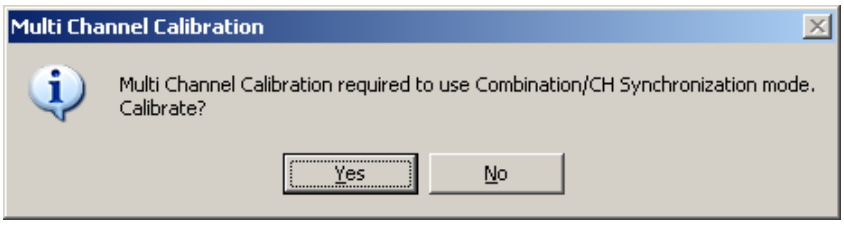


Figure 5.8-1 Multi Channel Calibration Requirement Message

Click [Next] after confirming the explanation. Calibration requires about 2 to 3 minutes. When clicking [No], refer to Figure 5.8-7 and Figure 5.8-8.

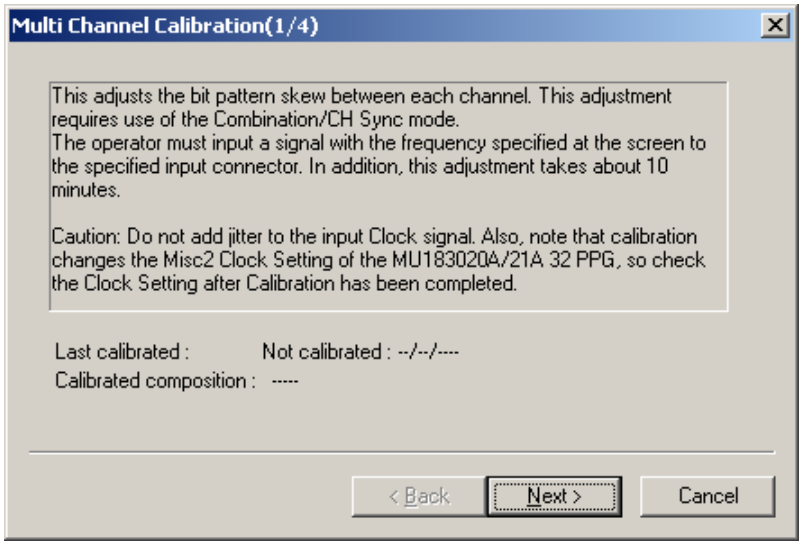


Figure 5.8-2 Multi Channel Calibration Screen 1

Connect the clock source and the MU183020A/MU183021A with the coaxial cables, input the clock frequency specified on the screen, and then click [Next].
When the MU181000A/B synthesizer is installed in the same main frame as the MU183020A/MU183021A, input the clock from the MU181000A/B to the MU183020A/MU183021A, for the MU181000A/B is used as a clock source automatically.

Notes:

- Do not impose jitter on the clock signal for input.
- If the MU181000A/B and MU181500B Jitter Modulation Source are installed in the same main frame as the MU183020A/MU183021A, change the Misc2 Clock setting so that the MU181000A/B will be a clock source automatically. Check the clock setting after the completion of Multi Channel Calibration.
- If the MU183020A/MU183021A is linked with the MU181000A/B, see Section 3.2.1 “Connecting with MU183040A” for clock signal connection.
- If the MU183020A/MU183021A is linked with the MU181000A/B and MU181500B, see Section 3.2.2 “Adding Jitter to Output Signal” for clock signal connection.
- When using external clock, see Section 3.2.3 “Using External Clock” for clock signal connection.
- If two or more MU183020A units are installed, click **Channel Synchronization**, and then click **CH Sync**, referring to Section 5.7 “Inter-module Synchronization Function”. Then, connect the clock source and the Ext Clock Input connector of each PPG by using coaxial cables with the same length.
- Calibration should be performed at the ambient temperature range of 20 to 30°C.

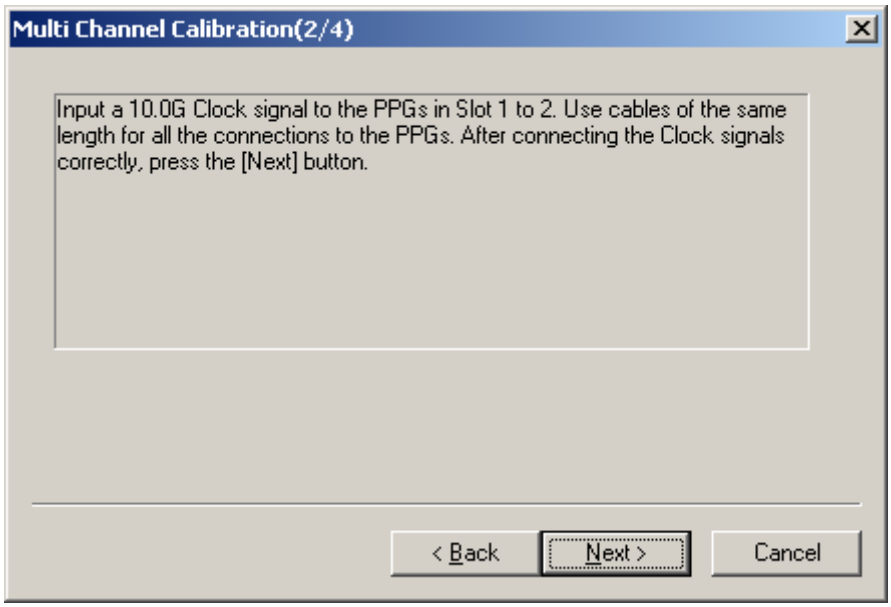


Figure 5.8-3 Multi Channel Calibration Screen 2

The calibration progress is displayed by the bar.

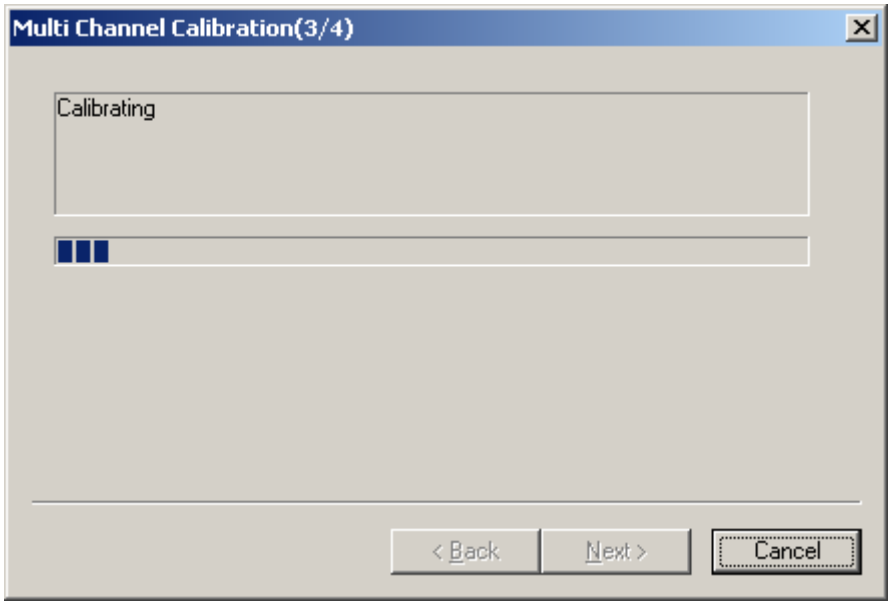


Figure 5.8-4 Multi Channel Calibration Screen 3

If the message dialog shown in Figure 5.8-5 is displayed during calibration, change the input clock frequency as indicated and click **OK**. Moreover, when both the MU183020A/21A and MU181000A/B synthesizer are installed in the same main frame, it is not necessary to change the frequency.

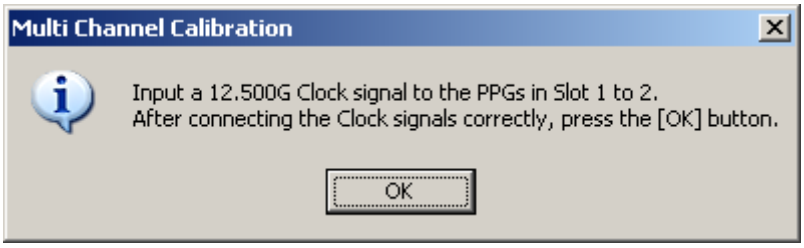


Figure 5.8-5 Clock Frequency Change Message

When the screen shown in Figure 5.8-6 appears, click [Finish] to complete the calibration.

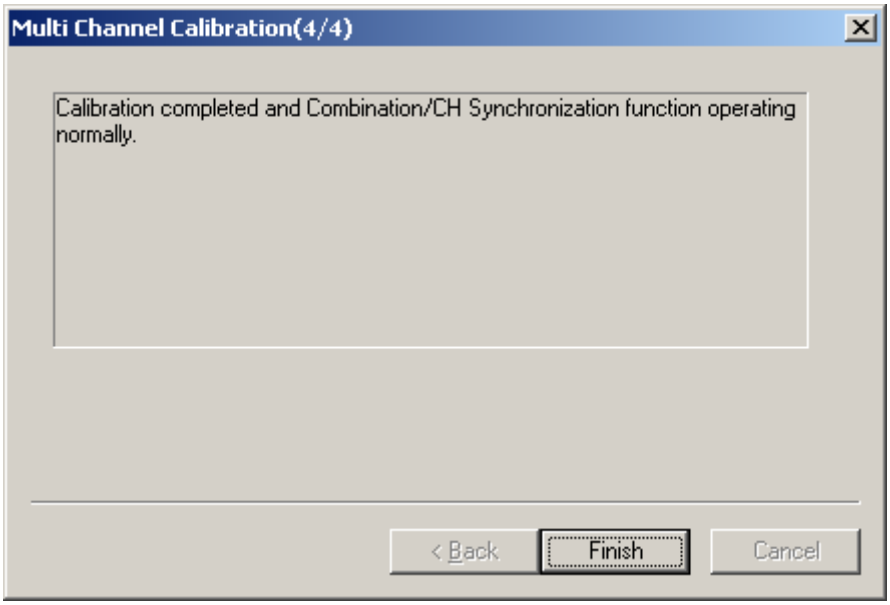


Figure 5.8-6 Multi Channel Calibration Screen 4

If [No] is clicked in the message dialog shown in Figure 5.8-1, click the **File** menu (Figure 5.8-7), and then click **Multi Channel Calibration**.

When [No] is clicked, the dialog shown in Figure 5.8-8 is displayed; if the check box is selected, this calibration-required dialog box will not appear again when calibration is required in future.

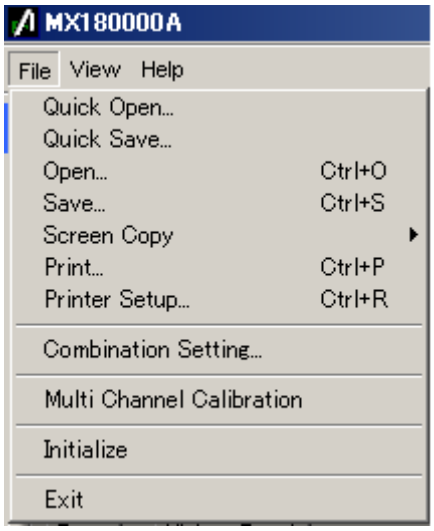


Figure 5.8-7 File Menu

Figure 5.8-8 Calibration Cancel Confirmation Dialog Box

After calibration has been completed once, it is not required again if the configuration of modules installed in the main frame is not changed. (Refer to the note in this page.)

To confirm whether or not calibration has already been performed, check the Calibration screen (Figure 5.8-9).

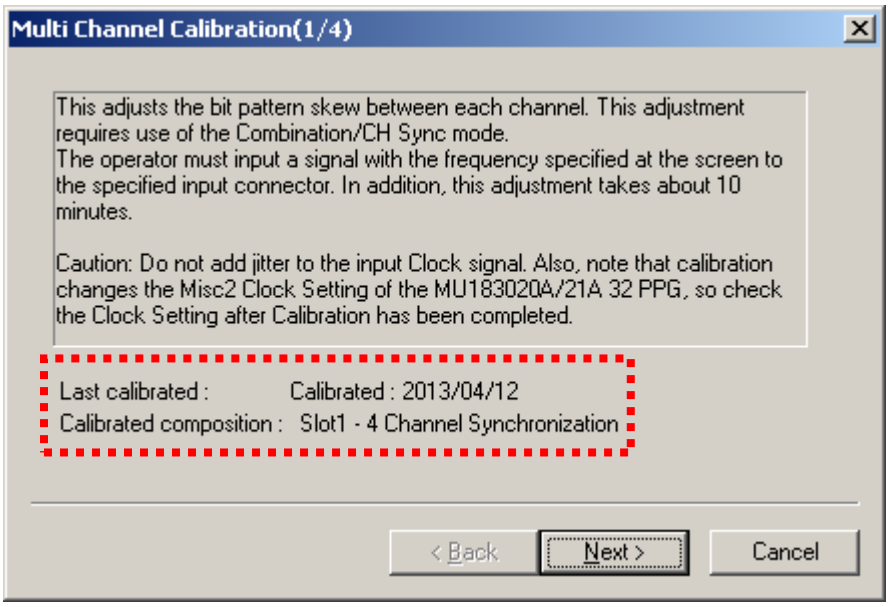


Figure 5.8-9 Calibration Execution Verification

Note:

When executing calibration for all channels of the MU183020A/MU183021A installed in the main frame, re-calibration is not required unless the module configuration is changed. However, it may be necessary to perform calibration several times depending on the selection of Channel Synchronization, Combination, or Inter-module Synchronization function.

5.8.1 How to perform multi channel calibration

This subsection describes how to perform multi channel calibration for typical module configurations after initialization. For more information about clock signal connection, refer to Section 3.2 “Inter-Module Connection”.

(1) Two MU183021A units and Synthesizer

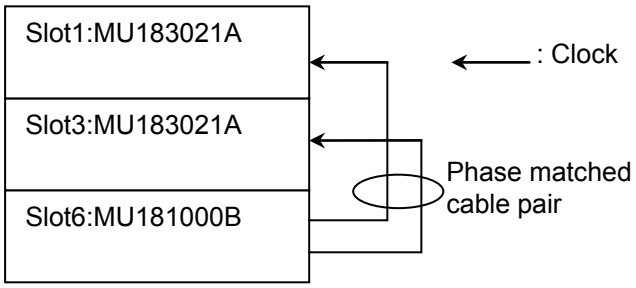
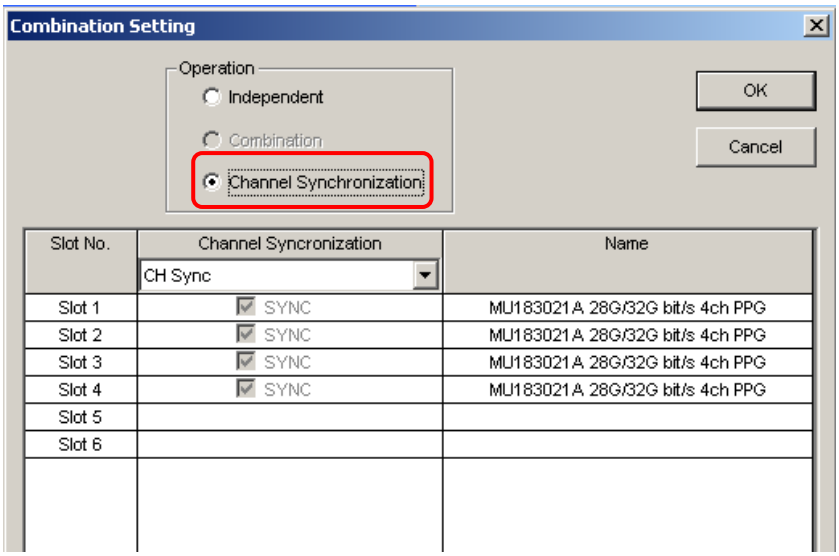


Figure 5.8.1-1 Example Clock Connection 1

1. Click the **Combination Setting** button in the module function button bar.

2. In the **Combination Setting** dialog box, click **Channel Synchronization**, and then click **CH Sync**.



3. When the **Multi Channel Calibration** dialog box appears as shown in Figure 5.8-1, perform the calibration according to the description of Figure 5.8-1 through Figure 5.8-6.

(2) MU183021A, Synthesizer, and Jitter Modulation Source

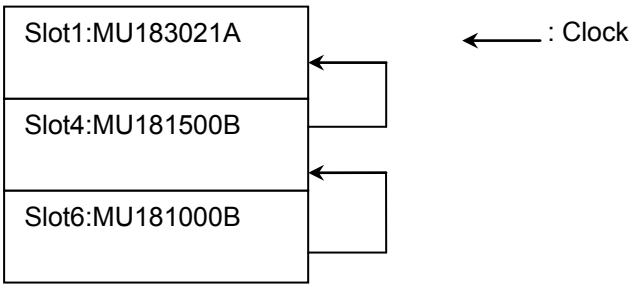
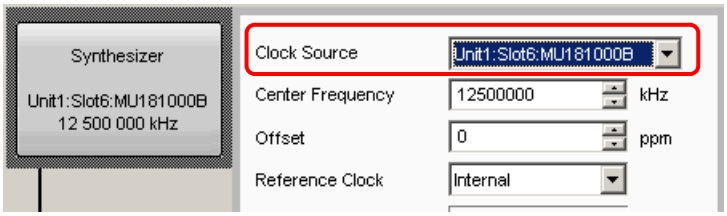
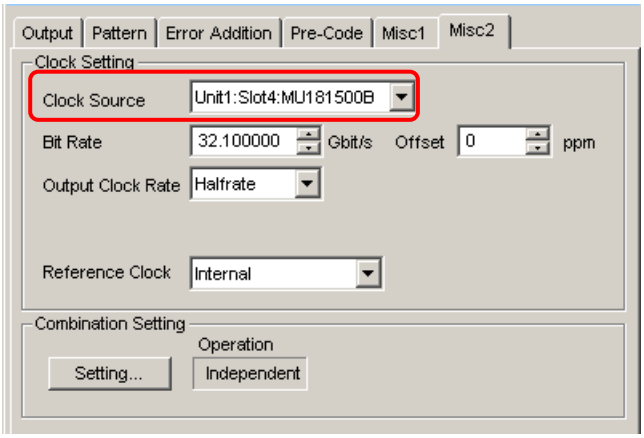


Figure 5.8.1-2 Example Clock Connection 2

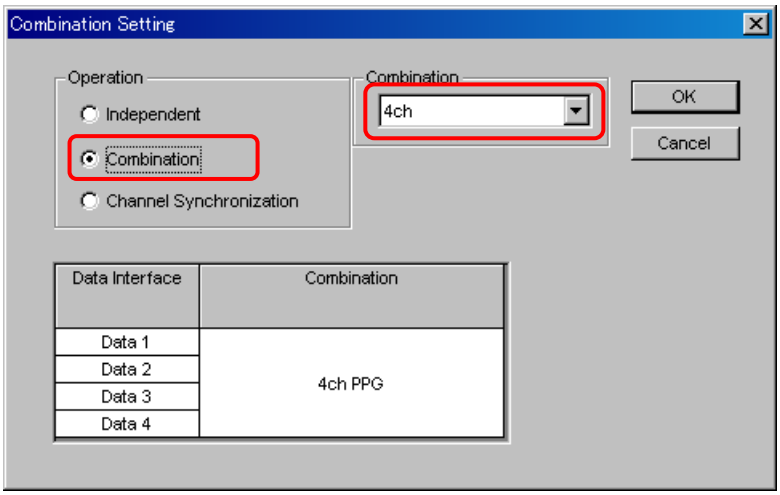
1. On the screen of the Jitter Modulation Source installed in Slot 4, click **Synthesizer** to display the clock setting screen. Click **Unit1:Slot6 MU181000B** in the **Clock Source** box.



2. On the screen of the MU183021A installed in Slot 1, click the **Misc2** tab. Click **Unit1:Slot4 MU181500B** in the **Clock Source** box.



3. To set the clock source, click [Setting…] under **Combination Setting** and open the **Combination Setting** dialog box. In the **Combination Setting** dialog box, click **Combination** under **Operation**, and click **4ch** in the **Combination** box.



4. When the **Multi Channel Calibration** dialog box appears as shown in Figure 5.8-1, perform the calibration according to the description of Figure 5.8-1 through Figure 5.8-6.

(3) Two MU183020A (Opt-23) units, Jitter Modulation Source, and External Synthesizer

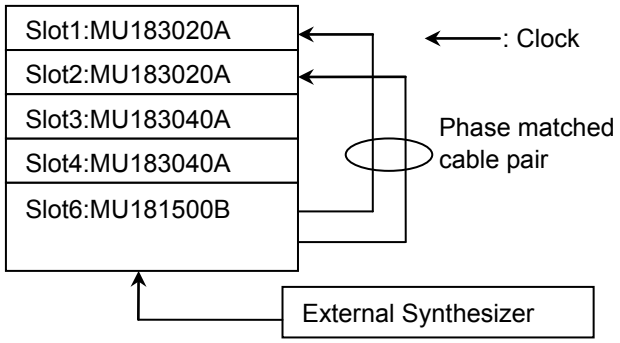
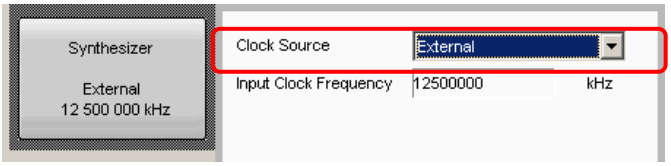


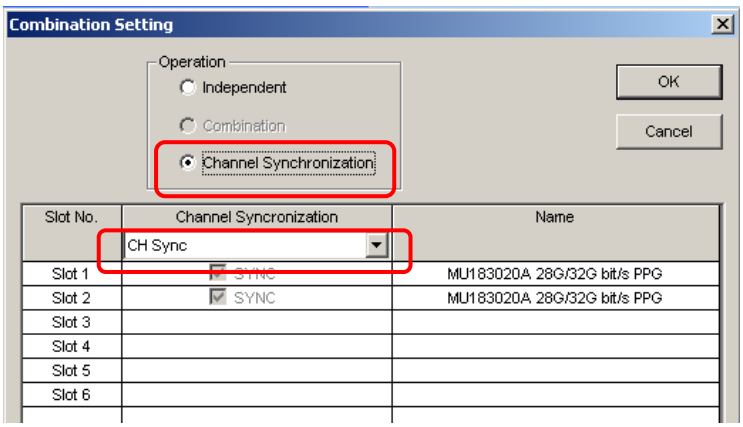
Figure 5.8.1-3 Example Clock Connection 3

1. On the screen of the Jitter Modulation Source installed in Slot 6, click **Synthesizer** to display the clock setting screen. Click **External** in the **Clock Source** box.



2. Click the **Combination Setting** button in the module function button bar.

3. In the **Combination Setting** dialog box, click **Channel Synchronization**, and then click **CH Sync**.



4. When the **Multi Channel Calibration** dialog box appears as shown in Figure 5.8-1, perform the calibration according to the description of Figure 5.8-1 through Figure 5.8-6.

5.9 Unit Sync Function

The Unit Sync function is used to synchronize multiple MP1800A units to generate the same pattern. This section explains how to set the Unit Sync function as well as the operations and restrictions when using this function.

5.9.1 Unit Sync Operation and Restrictions

The Unit Sync function synchronizes multiple main frames by sharing a timing signal between them.

Patterns can be generated and synchronized for up to 32ch by using both the Unit Sync function and the Channel Synchronization functions for synchronizing modules in the main frame.

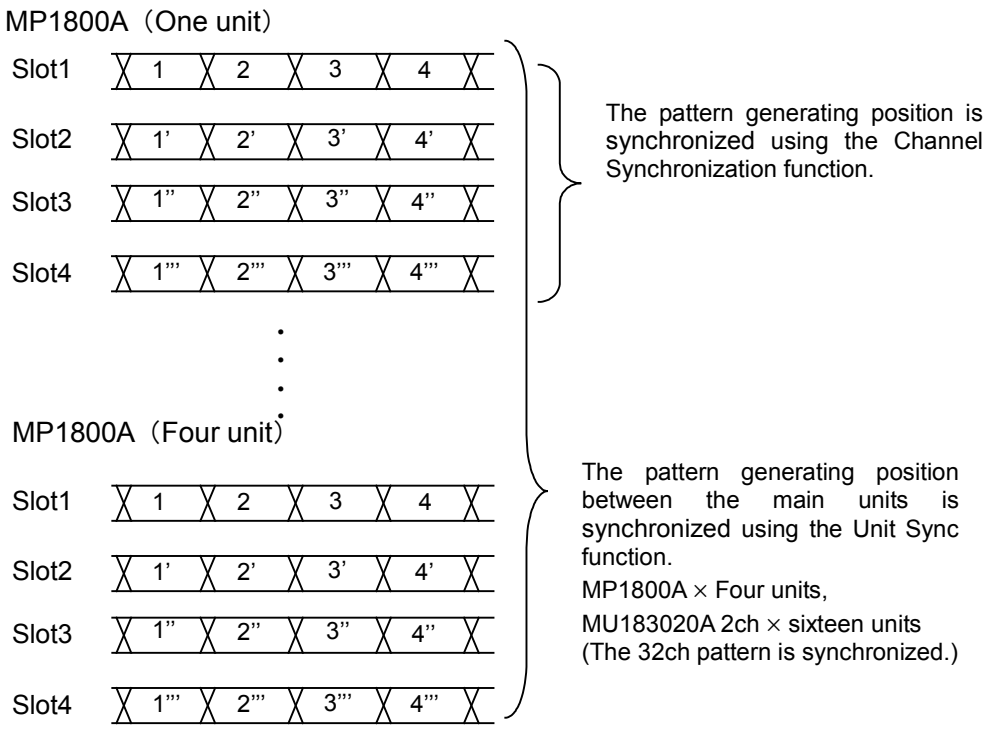


Figure 5.9.1-1 Channel Synchronization Pattern Generation

Since the Unit Sync function has a maximum bit phase error of ±128 bits between main frames, the adjustment is required to remove this bit phase error. Refer to Appendix E “Preparing to Use Unit Sync Function” for this adjustment procedure.
However, this bit phase error does not change unless the operation clock changes. The adjustment is required if the operation clock input is interrupted or changed.

Furthermore, there are following restrictions when using the Unit Sync function:

- Cannot use the Burst function
- Cannot add error using the external signal
- The Unit Sync function is unavailable if the MU183020A 1ch PPG (option x11/13) is installed.
- The Unit Sync function is unavailable if the MU183020A 2ch PPG and MU183021A 4ch PPG are used together.
- The Unit Sync function is unavailable if the MU181020A/B and MU183020A/21A are used together.

5.9.2 Unit Sync Setting

To use the Unit Sync function, click the Combination Setting button in the module function button bar, and set at the Combination Setting screen.

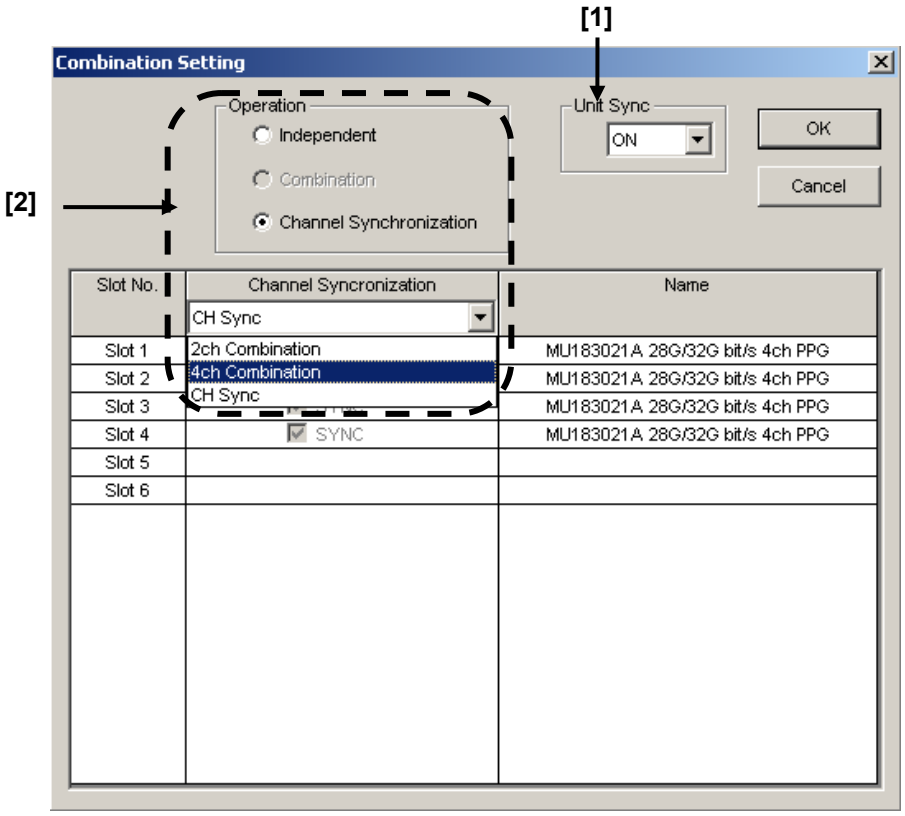


Figure 5.9.2-1 Combination Setting screen

[1] Sets Unit Sync function to ON/OFF
Set **Unit Sync** to **ON** and press **OK** to enable the function. Confirmed the message dialog (Figure 5.9.2-2) displayed according to the restrictions in section 5.9.1 when settings are changed.

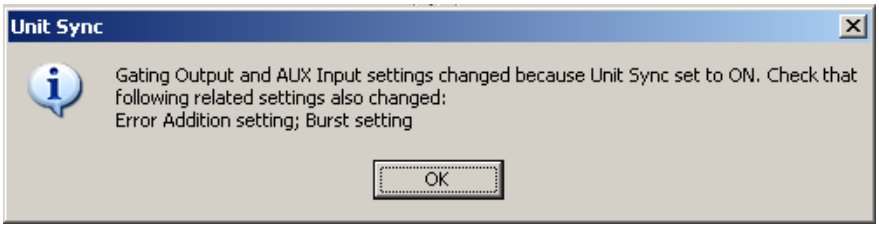


Figure 5.9.2-2 Dialog screen when settings changed at Unit Sync ON

When Unit Sync is ON, the combinations that can be set when Operation is set to either Combination or Channel Synchronization are shown in Table 5.9.2-1.

Table 5.9.2-1 Combination Settings for Unit Sync

Operation	Combination
Channel Synchronization	4ch
	2ch
	CH Sync

5.9.3 How to Use Unit Sync Function

This section explains how to use the Unit Sync function. Refer to Appendix E "Preparing to Use Unit Sync Function" for the connections and adjustment procedure when using the Unit Sync function.

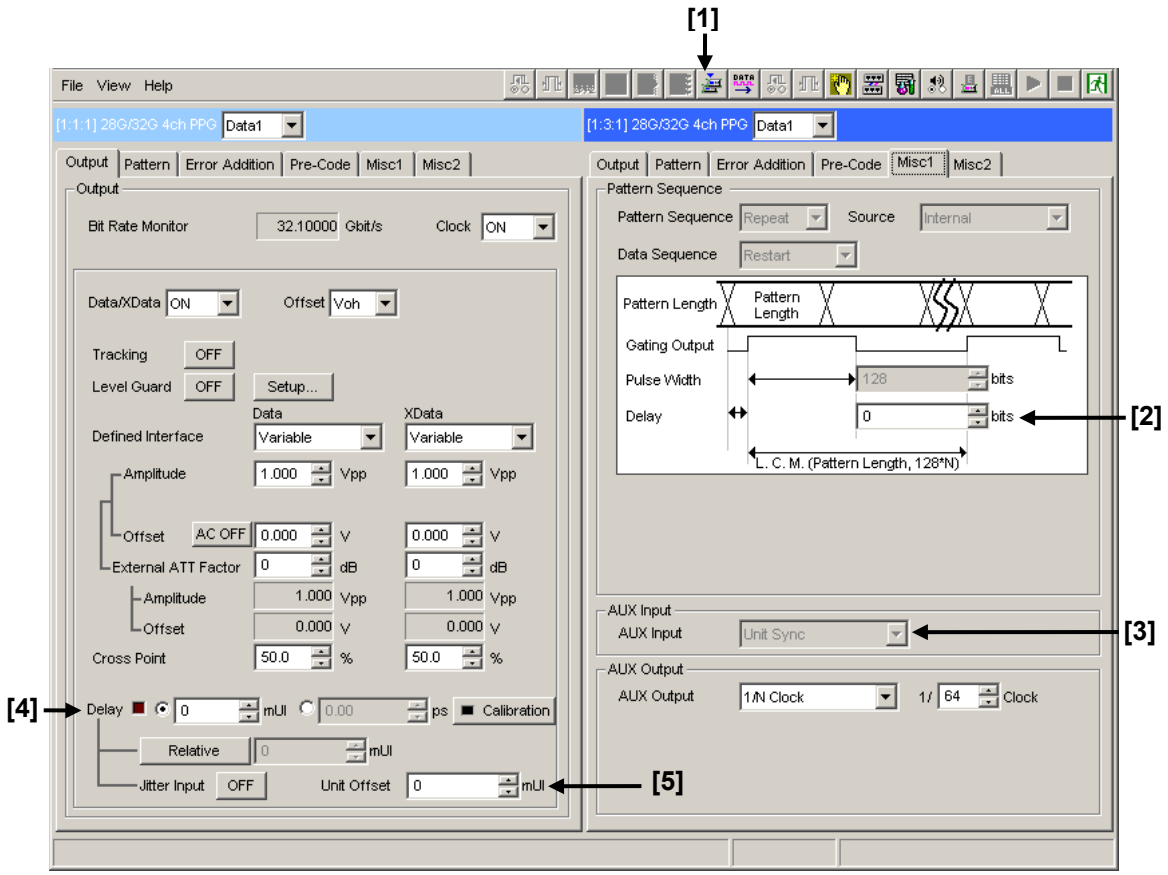


Figure 5.9.3-1 MX180000A Screen

[1] **Unit Sync Output** module function button
Outputs the timing signal for synchronization with the main frame. This button is available only when **Unit Sync** is set to **ON**.

Note:

Resynchronization must be performed again by clicking the button if the operation clock input is interrupted or changed. In addition, it is necessary to adjust the bit skew with the main frame after performing resynchronization.

[2] Gating Output Delay

This sets and adjusts the delay of the timing signal for synchronizing the main frames. The setting resolution is as follows:

Independent/CH Sync: 128-bit step
2ch Combination: 256-bit step
4ch Combination: 512-bit step

[3] AUX Input

This is a dedicated input for the timing signal for synchronizing the main frames when **Unit Sync** is set to **ON**.

[4] Delay

This adjusts the bit skew of the output pattern between channels by setting the Delay for each MU183020A/21A inserted in slots 1 to 4 of the same main frame.

[5] Unit Offset

This sets the offset for the delay at each main frame by adjusting the bit skew of the output pattern between main frames. The setting ranges are as follows, but there are some restrictions depending on the setting of Delay [4].

Independent:

–1000 to +1000 mUI = Delay setting + Unit Offset setting range

Channel Synchronization/Combination:

–128000 to +128000 mUI = Delay setting +
Unit Offset setting range

Chapter 6 Usage Examples

This chapter describes usage examples of measurement using the MU183020A/MU183021A.

6.1 Measuring Optical Transceiver Module

This section describes how to test the electrical interface input sensitivity of a CFP2 optical transceiver module by using MU183021A and MU183041A.

In the following test example, the MU183021A and MU182041A are mounted onto the MP1800A. The options configuring the test system are as follows:

MP1800A-014

MU181000A

MU183021A-x12

MU183041A

Measurement

1. Connect the MP1800A and DUT to GND.
2. Use a coaxial connector to connect the Clock Output connector of the MU181000A and the Ext. Clock Input connector of the MU183021A.
3. Use a coaxial connector to connect the Clock Output connector of the MU183021A and the Ext. Clock Input connector of the MU183041A.

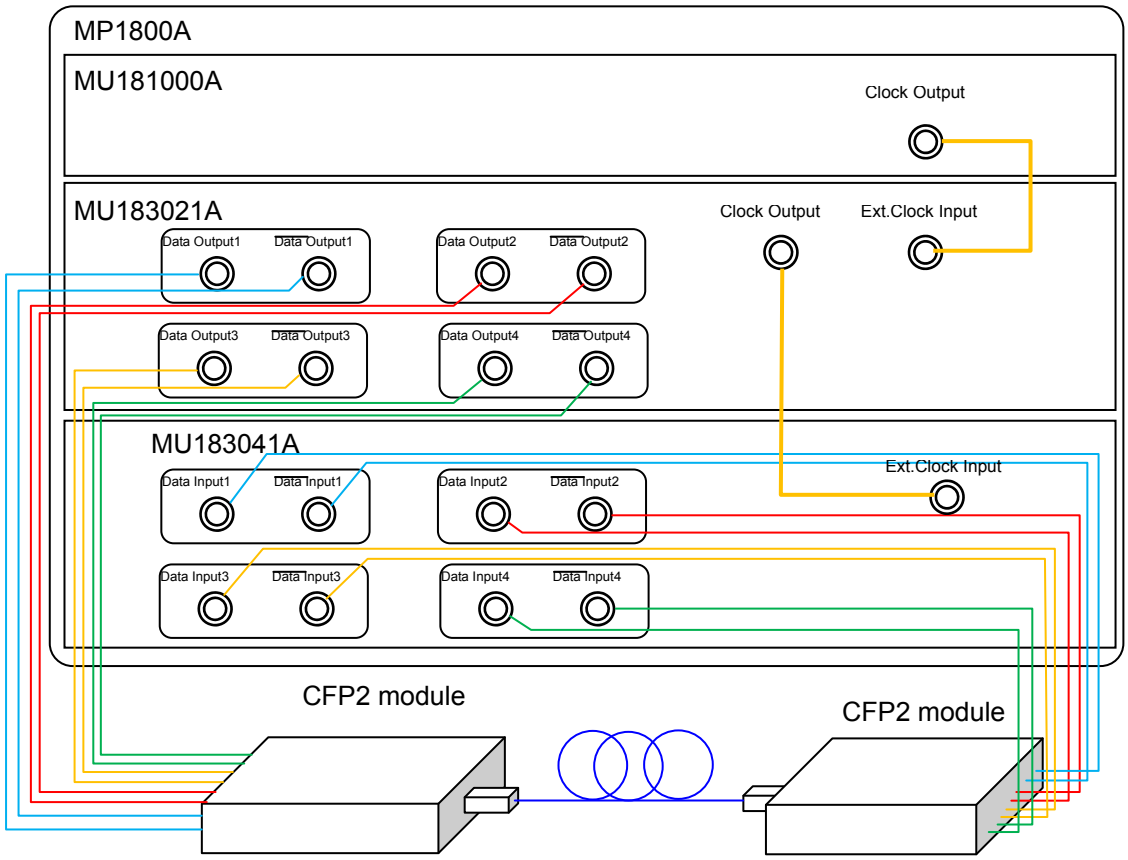


Figure 6.1-1 Connection diagram for CFP2 module evaluation

4. Use coaxial cables to connect the Data Output 1-4 connectors and $\overline{\text{Data}}$ Output 1-4 connectors of the MU183021A to the Data Input connectors of the CFP2 module (8 connections).
5. Use coaxial cables to connect the Data Input 1-4 connectors and $\overline{\text{Data}}$ Input 1-4 connectors of the MU183041A to the Data Output connectors of the CFP2 module (8 connections).

Test method

1. Connect the power cord of the MP1800A.
2. Turn on the MP1800A.
3. Turn off the Output module function button.
   Adjust the data output interface of the MU183021A to the input interface of the DUT. In the MU183021A Output tab, select Data/XData, and set Tracking to ON. The Data/XData amplitude and offset settings are applied commonly.
4. Set the pattern by selecting a test pattern in the Pattern tab of the MU183021A and MP183041A.
5. Set the operation bit rate at the Bit Rate Setting spin box in the Output tab of the MU183021A.
6. Adjust the data input interface of the MU183041A to the output interface of the DUT.
   Select a terminal condition at the Input Condition in the Input tab of the MU183041A. Since the CFP2 module is connected by the differential interface, select "Differential 100 Ohm," and then "Tracking."
7. Turn on the CFP2 module.
   Be sure to turn on the MP1800A first, and then the CFP2 module.

⚠ CAUTION

The DUT may be damaged if a signal line is connected or disconnected while the output is ON. Be sure to turn off the MP1800A before changing the cable connection.

8. Set Data/XData to ON in the Output tab of the MU183021A, and then select the Output module function button.
9. Adjust the threshold voltage of the MU183041A.
   Select the Auto Adjust module function button.
10. Start the measurement on the Result screen of the MU183041A, and check the BER measurement result.

11. After checking that the DUT is operating normally, the CFP2 module data input (TD+ and TD–) sensitivity can be measured by decreasing the output level of the MU183021A.

6.2 Generating 56 Gbit/s DQPSK Signals

This section describes how to generate 56G band DQPSK signals by using the MU183020A-x23 and the DQPSK modulator.

In the following test example, the MU183020A is mounted onto the MP1800A. The options configuring the test system are as follows:

MP1800A-014

MU181000A

MU183020A-x23

Measurement

1. Connect the MP1800A and DUT to GND.
2. Use a coaxial connector to connect the Clock Output connector of the MU181000A and the Ext. Clock Input connector of the MU183020A.
3. Use coaxial cables to connect the Data Output 1 and 2 and $\overline{\text{Data}}$ Output 1 and 2 connectors of the MU183020A to the DQPSK modulator (four connections).

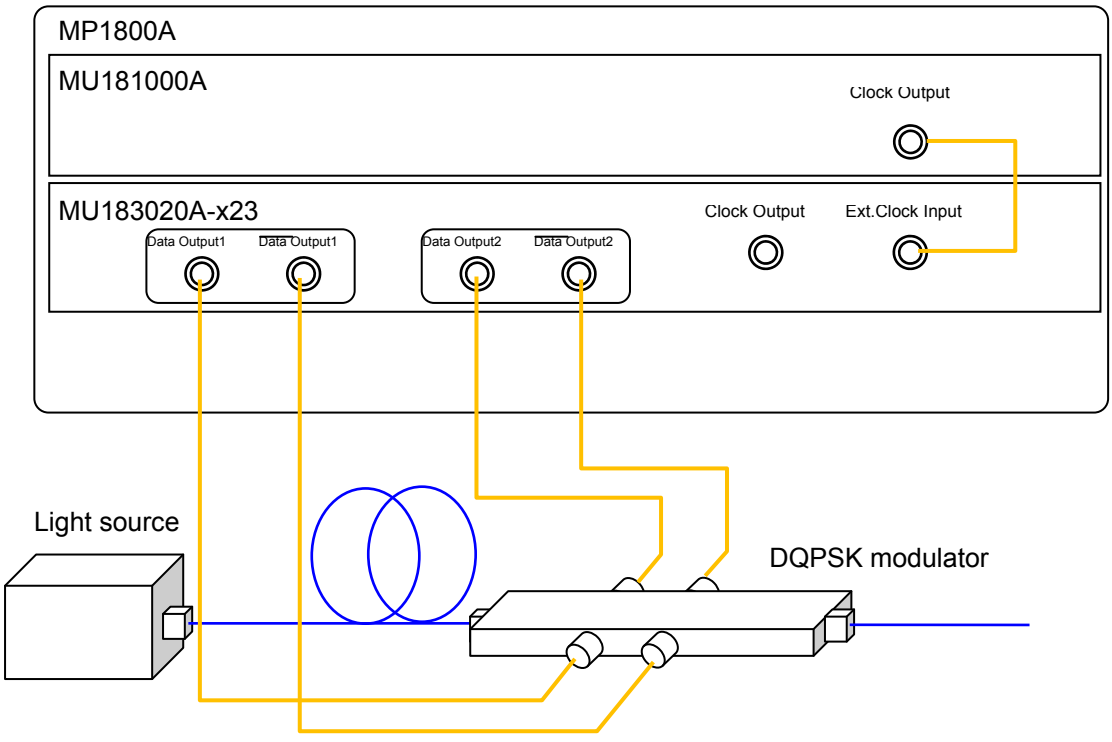


Figure 6.2-1 Connection diagram for generating 56Gbit/s DQPSK signals

Test method

1. Connect the power cord of the MP1800A.
2. Turn on the MP1800A.
3. Adjust the data output interface of the MU183020A to the input interface of the DUT. In the MU183020A Output tab, select Data/XData, and set Tracking to ON. The Data/XData amplitude and offset settings are applied commonly.
4. Set the operation bit rate to 28 Gbit/s at the Bit Rate Setting spin box in the Output tab of the MU183020A.
5. Select a test pattern in the Pattern tab of the MU183020A.
6. Set “2ch Combination” at the Combination in the Misc2 tab of the MU183020A.
7. In the Pre-Code tab of the MU183020A, select DQPSK in the Type dropdown list.
8. Set Data/XData to ON in the Output tab of the MU183020A, and then select the Output module function button.

By adding MU183020A signals to the DQPSK modulator, optical signals modulated to 56 Gbit/s are outputted.

Chapter 7 Remote Command

For the explanation of the SCPI format and status, refer to the *MX180000A Signal Quality Analyzer Control Software Operation Manual Remote Control.*

For remote control commands of MU183020A, refer to Section 7.11 “28G/32G bit/s PPG Commands” in the *MX180000A Signal Quality Analyzer Control Software Operation Manual Remote Control*.

Chapter 8 Performance Test

This chapter describes the performance testing of the MU183020A/MU183021A.

8.1 Performance Test Items

Performance test is executed to check that the major functions of the MU183020A meet the required specifications.
Execute performance test at acceptance inspection, operation check after repair, and periodic testing (once every six months).

8.2 Devices Required for Performance Tests

Before starting performance test, warm up the MU183020A and the measuring instruments for at least 30 minutes. Table 8.2-1 shows the required devices for performance test.

Table 8.2-1 Devices Required for Performance Tests

Device name	Required performance
Error detector (MP1800A + MU183040A-x01)	Operating frequency: 2.4 to 32.1 GHz Data input sensitivity: 300 mVp-p or more
Sampling oscilloscope	Electrical interface: 70 GHz or more band
Signal generator (MP1800A + MU181000A/B or MG3690 series)	When using Ext Clock: Operating frequency: 1.2 to 16.05 GHz Output level: 300 to 1000 mVp-p Waveform: Rectangular wave or sine wave
J1439 coaxial cables (80 cm K connector)	Bandwidth: 40 GHz
J0541E Coaxial Attenuator	6 dB Attenuation

Note:

Before starting the performance test, warm up the device under test and the measuring instruments for at least 30 minutes, and wait until they become sufficiently stabilized unless otherwise specified.

Maximum measurement accuracy is assured under the following conditions:
Measurement is performed at room temperature.
Fluctuations of AC power supply voltage are small.
Noise, vibration, dust, and humidity are insignificant.

8.3 Performance Test Items

This section describes the following test items.

(1) Operating bit rate range

(2) Waveform

8.3.1 Operating frequency range

(1) Specifications

Table 8.3.1-1 Specifications

Option	Specifications
MU183020A	2.4 to 28.1 Gbit/s
MU183020A-x01	2.4 to 32.1 Gbit/s
MU183021A	2.4 to 28.1 Gbit/s
MU183021A-x01	2.4 to 32.1 Gbit/s

(2) Device connection

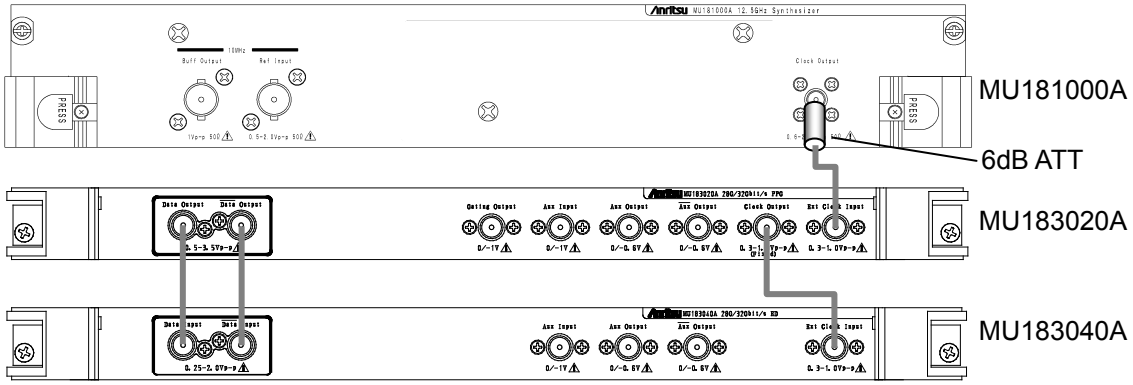


Figure 8.3.1-1 Connection diagram for operating frequency range test

When using the MU181000A, attach the 6 dB Coaxial Attenuator to the Clock Output connector.

(3) Test procedure

1. Mount the MU183020A onto the MP1800A, and turn on the MP1800A with the cables unconnected.
2. Set the Data signal output amplitude of the MU183020A to 500 mVp-p, offset (Vth) to 0 V, test pattern to PRBS 31, and mark ratio to 1/2.
3. Turn off the MP1800A when setting the parameters completely.
4. Connect the measuring instrument cables as shown in Figure 8.3.1-1.
5. Turn on the MP1800A and the measuring instruments, and warm them up.
6. After warming up the instruments, enable the MP1800A signal output (ON) to output signals from the MU183020A.
7. Adjust the phase and threshold voltage of the MU183040A to the optimum values.
8. Check that no error is detected by the MU183040A.
9. Change the operating frequency and check if no error occurs within the rated operating frequency range.

8.3.2 Waveform Evaluation Test

(1) Specifications

Table 8.3.2-1 Specifications for MU183020A

Item	Specification	
	Option x12/x22	Option x13/x23
Amplitude	0.5 to 2.0 Vp-p	0.5 to 3.5 Vp-p
Offset (Voh)	−2.0 to +3.3 V	
Cross point	Amplitude: 0.5 to 0.998 Vp-p 30 to 70% Amplitude: 1.0 to 2.0 Vp-p 20 to 80%	Amplitude: 0.5 to 0.998 Vp-p 30 to 70% Amplitude: 1.0 to 3.5 Vp-p 20 to 80%
Tr/Tf	12 ps (20 to 80%)*1,*2,*3	
Jitter	8 ps p-p*1,*3,*4	

*1: If Option x01 is not available, then this is at 28.1 GHz.
If Option x01 is available, then this is at 32.1 GHz.

*2: For Option x12 and x22, Amplitude is 2.0 Vp-p.
For Option x13 and x23, Amplitude is 3.5 Vp-p.

*3: Typical value

*4: The jitter specification value is defined assuming that the oscilloscope with residual jitter less than 200 fs (RMS) is used.

Table 8.3.2-2 Specifications for MU183021A

Item	Specification	
	Option x12	Option x13
Amplitude	0.5 to 2.0 Vp-p	0.5 to 3.5 Vp-p
Offset (Voh)	−2.0 to +3.3 V	
Cross point	Amplitude: 0.5 to 0.998 Vp-p 30 to 70% Amplitude: 1.0 to 2.0 Vp-p 20 to 80%	Amplitude: 0.5 to 0.998 Vp-p 30 to 70% Amplitude: 1.0 to 3.5 Vp-p 20 to 80%
Tr/Tf	12 ps (20 to 80%)*1,*2,*3	
Jitter	8 ps p-p*1,*3,*4	

*1: If Option x01 is not available, then this is at 28.1 GHz.
If Option x01 is available, then this is at 32.1 GHz.

*2: For Option x12, Amplitude is 2.0 Vp-p.
For Option x13, Amplitude is 3.5 Vp-p.

*3: Typical value

*4: The jitter specification value is defined assuming that the oscilloscope with residual jitter less than 200 fs (RMS) is used.

(2) Device connection

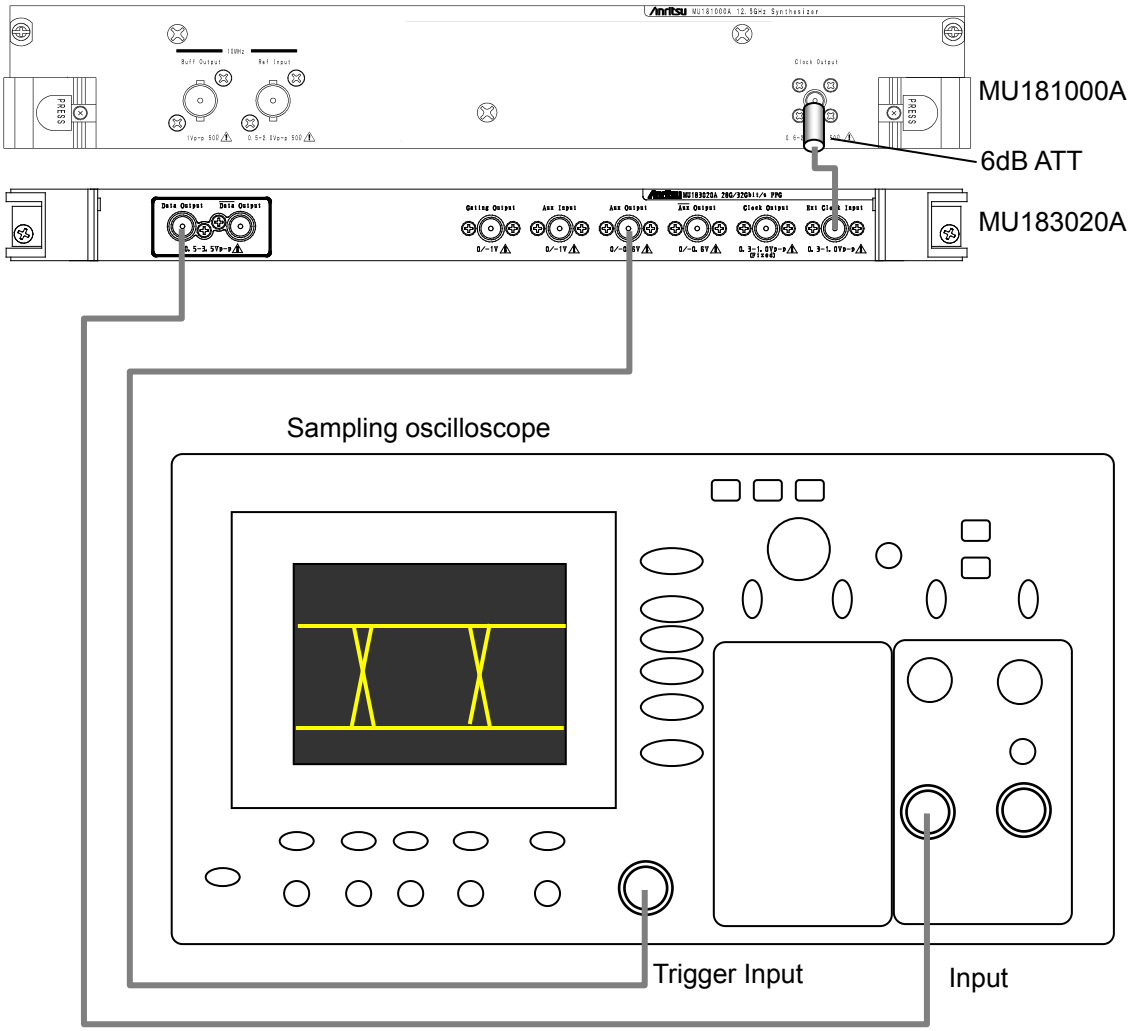


Figure 8.3.2-1 Connection diagram for waveform test

When using the MU181000A, attach the 6 dB Coaxial Attenuator to the Clock Output connector.

(3) Test procedure

1. Mount the MU183020A onto the MP1800A, and turn on the MP1800A with the cables unconnected.
2. Set the Data output amplitude, offset, and cross point to be tested in the MU183020A Output tab window.
3. Set the test pattern in the Pattern tab of the MU183020A.

   Since the specification parameters are evaluated by the eye pattern observation, set the test pattern to PRBS 31, and the mark ratio to 1/2.

4. Select a trigger signal to input to the oscilloscope. Select 1/N Clock in the AUX Output dropdown list in the Misc1 tab of the MU183020A, and set the division ratio according to the sampling oscilloscope used.
5. Turn off the MP1800A when setting the parameters completely.
6. Connect the measuring instrument cables as shown in Figure 8.3.2-1.
7. Turn on the MP1800A and the measuring instruments, and warm them up.
8. After warming up the instruments, enable the MP1800A signal output (ON) and output signals.
9. Observe the output waveform on the sampling oscilloscope, and check that all the items meet the specifications.
10. Use a coaxial cable to connect the XData Output connector of the MU183020A and the Input connector of the sampling oscilloscope. Repeat the observation in Step 9.
11. If there are multiple channels, repeat the observation in Step 9 for all Data Output and XData Output.

Chapter 9 Maintenance

This chapter describes the maintenance of the MU183020A.

9.1 Daily Maintenance

Wipe off any external stains with a cloth damped with diluted mild detergent.
Vacuum away any accumulated dust or dirt with a vacuum cleaner.
Tighten any loose parts fixed with screws, using the specified tools.

9.2 Cautions on Storage

Wipe off any dust, soil, or stain on the MU183020A prior to storage. Avoid storing the MU183020A in any of the following locations:

- In direct sunlight for extended periods
- Outdoors
- In excessively dusty locations
- Where condensation may occur
- In liquids, such as water, oil, or organic solvents, and medical fluids, or places where these liquids may adhere
- In salty air or in place chemically active gases (sulfur dioxide, hydrogen sulfide, chlorine, ammonia, nitrogen dioxide, or hydrogen chloride etc.) are present
- Where toppling over may occur
- In the presence of lubricating oil mists
- In places at an altitude of more than 2,000 m
- In the presence of frequent vibration or mechanical shock, such as in cars, ships, or airplanes
- Under either of the following temperature and humidity conditions:
  Temperature range of ≤–20°C or ≥60°C
  Humidity range of ≥85%

Recommended storage conditions

In addition to the abovementioned storage cautions, the following environment conditions are recommended for long-term storage.

- Temperature range of 5 to 30°C
- Humidity range of 40 to 75%
- Slight daily fluctuation in temperature and humidity

9.3 Transportation

Use the original packing materials, if possible, when packing the MU183020A for transport. If you do not have the original packing materials, pack the MU183020A according to the following procedure. When handling the MU183020A, always wear clean gloves, and handle it gently so as not to damage it.

<Procedure>

1. Use a dry cloth to wipe off any stain or dust on the exterior of the MU183020A.
2. Check for loose or missing screws.
3. Provide protection for structural protrusions and parts that can easily be deformed, and wrap the MU183020A with a sheet of polyethylene. Finally, cover with moisture-proof paper.
4. Place the wrapped MU183020A into a cardboard box, and tape the flaps with adhesive tape. Furthermore, store it in a wooden box as required by the transportation distance or method.
5. During transportation, place it under an environment that meets the conditions described in Section 9.2 “Cautions on Storage”.

9.4 Calibration

Regular maintenance such as periodic inspections and calibration is essential for the Signal Quality Analyzer Series for long-term stable performance.
Regular inspection and calibration are recommended for using the Signal Quality Analyzer Series in its prime condition at all times. The recommended calibration cycle after delivery of the Signal Quality Analyzer Series is twelve months.

If you require support after delivery, contact an Anritsu Service and Sales office. Contact information can be found on the last page of the printed version of this manual, and is available in a separate file on the CD version.

We may not provide calibration or repair if any of the following cases apply.

- Seven or more years have elapsed after production and parts for the instrument are difficult to obtain, or it is determined that reliability cannot be maintained after calibration/repair due to significant wear.
- Circuit changes, repair, or modifications are done without our approval.
- It is determined that the repair cost would be higher than the price of a new item.

9.5 Disposal

Confirm the notes described in the Signal Quality Analyzer Series Installation Guide and observe national and local regulations when disposing of the MU183020A.

Chapter 10 Troubleshooting

This chapter describes how to check whether a failure has arisen when an error occurs during the operation of the MU183020A/MU183021A.

10.1 Problems Discovered during Module Replacement

Table 10.1-1 Remedies for problems discovered during replacement of module

Symptom	Location to Check	Remedy
A module is not recognized.	Is the module installed properly?	Install the module again by referring to Section 2.3 "Installing and Removing Modules" in the installation guide.
	Are the appropriate modules installed?	To check the appropriate modules and software version of the MU183020A, access to "MP1800 Series Signal Quality" on your Web site (http://www.anritsu.com). Right-click the "MP1800 Series Signal Quality" and you can access to your area website. If the appropriate modulus are not recognized, it may have failed. Contact an Anritsu Service and Sales office. Contact information can be found on the last page of the printed version of this manual, and is available in a separate file on the CD version.

10.2 Problems Discovered during Output Waveform Observation

Table 10.2-1 Remedies for problems discovered during waveform observation

Symptom	Location to Check	Remedy
Output waveform cannot be monitored normally.	Is the [Data/XData] or [Clock] on the Output tab window set to ON?	In the Output tab window, set [Data/XData] or [Clock] to be output to ON. When the module function button [Output ON/OFF] is enabled, click it to set to ON.
	Is module function button [Output ON/OFF] is set to ON?	Click the module function button [Output ON/OFF] to ON.
	Is the operating clock supplied normally?	When using the internal clock, check the bit rate setting. When the clock is supplied externally, check the connection interface. Refer to Section 3.1 "Panel Layout" for the interface.
	Is the trigger clock set correctly?	It is recommended to use the signal output from Aux output connector as the trigger clock. Check the Aux output connector settings and interface with the sampling oscilloscope to be measured.
	Is the electrical interface cable loose?	Tighten the connector.
	Do the cables used have good high-frequency characteristics?	Use cables or connectors with good high-frequency characteristics.

10.3 Problems Discovered during Error Rate Measurement

Table 10.3-1 Remedies for problems discovered during error rate measurement

Symptom	Location to Check	Remedy
An error occurs.	Is the connection interface with the DUT to be measured correct?	Check that the data rate, level, offset and termination conditions are the same.
	Are the logical patterns correctly set on the MU183020A and the MU183040A error detector (ED)?	Check if the patterns generated by the MU183020A are set such that they can be received by the DUT, and if the set patterns generated by the DUT and detected by the ED are the same. If the DUT outputs the patterns from the MU183020A as they are, connect the MU183020A and ED directly to check if an error is detected.
	Is the error addition function set to off?	Check that the [Error Addition] switch on the Error Addition screen is set to off.
	Is the electrical interface cable loose?	Tighten the connector.
	Do the cables used have good high-frequency characteristics?	Use cables or connectors with good high-frequency characteristics.
	Are sufficient phase margin and bias margin are secured?	Adjust the phase and offset to be optimal between the MU183020A and the DUT as well as between the DUT and ED, respectively.

If a problem cannot be solved using any of the items listed above, perform initialization and check the items again. If the problem still occurs, contact an Anritsu Service and Sales office. Contact information can be found on the last page of the printed version of this manual, and is available in a separate file on the CD version.

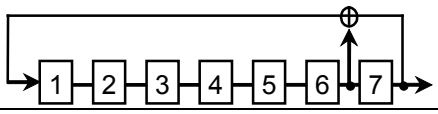
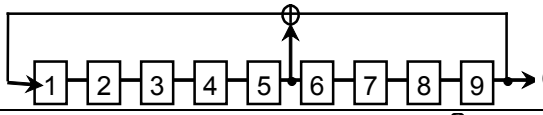
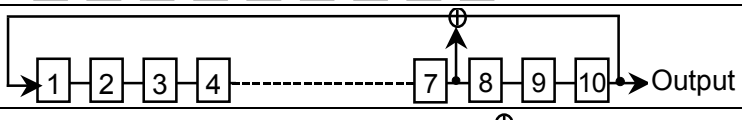
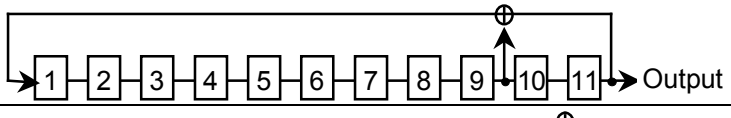
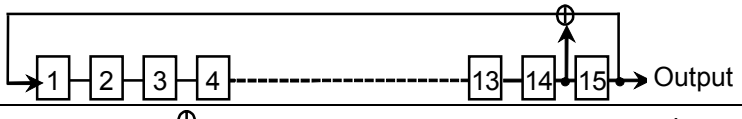
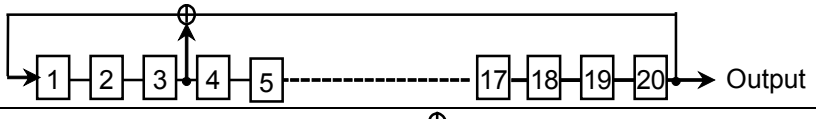
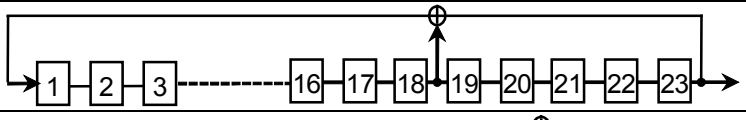
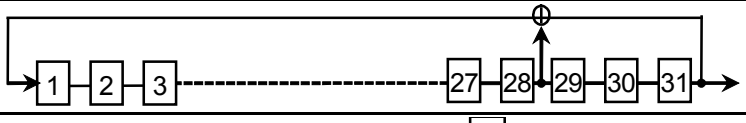
A.1 Pseudo-Random Pattern

Table A.1-1 shows the principle of pseudo-random pattern generation. A pseudo-random pattern is expressed in an N-th degree generating polynomial, with one cycle of 2^n-1. For a PRBS pattern with a cycle of 2^n-1, a pattern of successive "1s" for the number N is generated once in a cycle.

For the output level of the PRBS pattern, "1" indicates the low level and "0" indicates the high level when Logic is set to POS (positive).

The mark ratios of the PRBS pattern are generated as shown in the block diagrams of Table A.1-1.

Table A.1-1 Principle of pseudo-random pattern generation

Cycle	Generating polynomial	Pattern generation block diagram
2^7-1	$1+X^6+X^7$	
2^9-1	$1+X^5+X^9$	
$2^{10}-1$	$1+X^7+X^{10}$	
$2^{11}-1$	$1+X^9+X^{11}$	
$2^{15}-1$	$1+X^{14}+X^{15}$	
$2^{20}-1$	$1+X^3+X^{20}$	
$2^{23}-1$	$1+X^{18}+X^{23}$	
$2^{31}-1$	$1+X^{28}+X^{31}$	

N : Shift register (N=1, 2, 3….)

⊕ : Exclusive OR

B.1 List of Initialized Settings

This appendix shows the MU183020A settings that are initialized to the defaults at factory shipment.

In addition, All settings can be initialized using the Initialize pull-down from the File menu.

Table B.1-1 List of Initialized Items

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Output	Data/XData Output ON/OFF			ON
	Clock Output ON/OFF			ON
	Amplitude/Offset			Voh
	Data/ XData	Tracking		OFF
		Level Guard		OFF
		Level Guard Setup	Amplitude	1.000 Vp-p
			Offset limit	–4.000 to 3.300 V
		Defined Interface		Variable
			Amplitude	1.000 Vp-p
			Offset switching	AC OFF
			Offset	0.000 V
			External ATT Factor	0 dB
		Cross Point		50%
		Half Period Jitter		0
		Delay		0 mUI
			Calibration	–
		Jitter Input		OFF

Table B.1-1 List of Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Pattern	PRBS	Number of Rows PRBS steps		15
		Logic		POS
		Mark Ratio		1/2
	Zero-substitution	Number of Rows PRBS steps		15
		Zero-Substitution Length		1 bit
		Addition Bit		1
	Data	Data Pattern		2 bit At 2ch Combination: 4 bits At 4ch Combination: 8 bits
	Mixed Data	Logic		POS
		Block count		1
		Row Length		1536 bits At 2ch Combination: 3072 bits At 4ch Combination: 6144 bits
		Data Length		1024 bits At 2ch Combination: 2048 bits At 4ch Combination: 4096 bits
		Row count		1
		PRBS	Pattern	PRBS15
			Mark Ratio	1/2
		Scramble		OFF
		Scramble Setup		All OFF
		PRBS Sequence		Consecutive

Table B.1-1 List of Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Pattern (continued)	Pattern Editor	Zoom		×1
		Block count		1
		Row Length		1536 bits At 2ch Combination: 3072 bits At 4ch Combination: 6144 bits
		Data Length	Data	2 bits At 2ch Combination: 4 bits At 4ch Combination: 8 bits
			Mixed	1024 bits At 2ch Combination: 2048 bits At 4ch Combination: 4096 bits (When Mixed-Data is selected)
		Row count		1
Error Addition	Error Addition			OFF
		Source		Internal
		Variation		Repeat
		Route		Select, 1
		Error Rate		1E–3
		When Test Pattern is Mixed Row 1		Data:Unselected PRBS:Unselected
Pre-Code*	Pre-Code			
		ON/OFF selection		OFF
		Type		DQPSK
		Initial Data		1

*: This function is available for the MU183020A-x22, MU183020A-x23 and MU183021A.

Table B.1-1 List of Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Misc1	Pattern SequenceSetting			Repeat
		Repeat	Pulse Width	64 bits
			Delay	0
		Burst	Source	Internal
			Data Sequence	Restart
			Enable Period	128 000 bits 2ch Combination:Default×2 4ch Combination:Default×4
			Burst Cycle	12 800 000 bits 2ch Combination:Default×2 4ch Combination:Default×4
			Delay	0 bits
			Pulse Width	128 000 bits 2ch Combination:Default×2 4ch Combination:Default×4
	Aux Input			Error Injection
	Aux Output Setting			1/N Clock
		1/N Clock	(Devide ratio)	1/64 clock
		Pattern Sync	For PRBS, Zero-Substitution, Data Position	 1 bits
			For Mixed Data Block No. Row No.	 1 1
		Burst Output 2	Delay	0
			Pulse Width	128 000 bits 2ch Combination:Default×2 4ch Combination:Default×4

Table B.1-1 List of Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Misc2	Clock Setting			
		Clock Source		External
		Bit Rate		12.500 000 Gbit/s
		Offset		0 ppm
		Output Clock Rate		Half rate
		Reference Clock		Internal
		Operation Bit Rate		2.4 to 32.1
	Combination Setting			
		Operation		Independent
		Combination*		2ch
		Channel Synchronization*		Data1 and Data2 are SYNC.
	Grouping Setting	Grouping item setting		Data1-2 (MU183020A) Data1-4 (MU183021A)
		Output		OFF
		Pattern		OFF

Note:

When the Initialize function is executed in Combination or Channel Synchronization status, Independent, which is the initial status, is restored.

Appendix C Setting Restrictions

C.1 Restriction on Use of Other Modules

The following modules cannot be used concurrently when the MU183020A, MU183021A, MU183040A, or MU183041A is installed.

- MU181020A 12.5 Gbit/s PPG
- MU181020B 14 Gbit/s PPG
- MU181040A 12.5 Gbit/s ED
- MU181040B 14 Gbit/s ED

Note:

For MX180000A Installer Version 7.04.00 or after, simultaneous use is available among some combinations of 32Gbit/s PPG or ED and 12.5/14Gbit/s PPG or ED.For details, refer to the release notes.

C.2 Setting Restrictions

This appendix describes restrictions due to options or set parameters, and the conditions for using the Combination and Channel Synchronization functions.

C.2.1 Setting range of offset and amplitude

■Relationship between offset reference value and amplitude

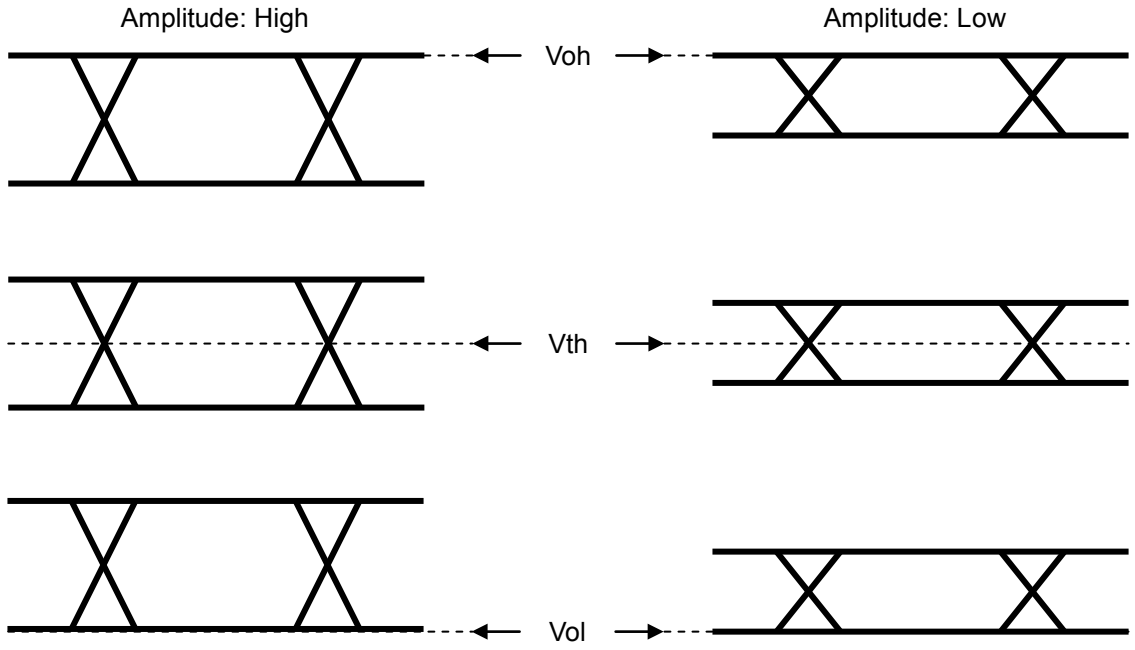


Figure C.2.1-1 Relationship between offset reference value and amplitude

C.2.2 Option x12/x22 Data Output (0.5 to 2.0 Vp-p)

Amplitude: 0.5 to 2.0 Vp-p

Offset: –2.0 to +3.3 V (Voh)

(a) When Voh is selected:

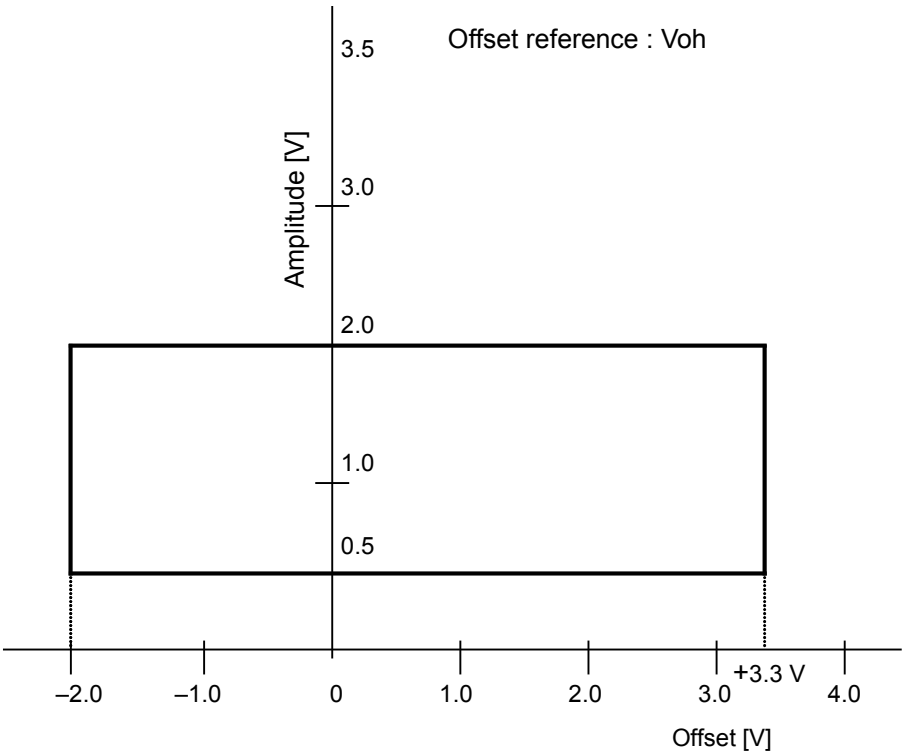


Figure C.2.2-1 MU183020A-x12/x22, MU183021A-x12
Setting range of amplitude and offset based on offset reference (Voh)

(b) When Vth is selected:

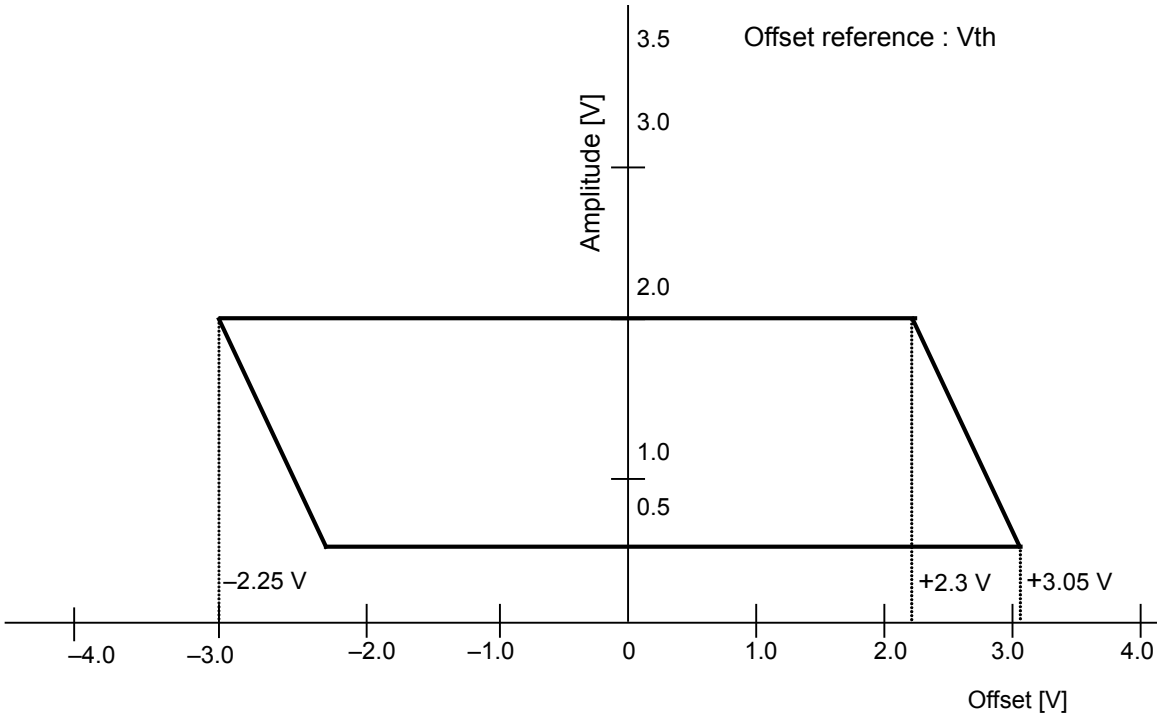


Figure C.2.2-2 MU183020A-x12/x22, MU183021A-x12
Setting range of amplitude and offset based on offset reference (Vth)

(c) When Vol is selected:

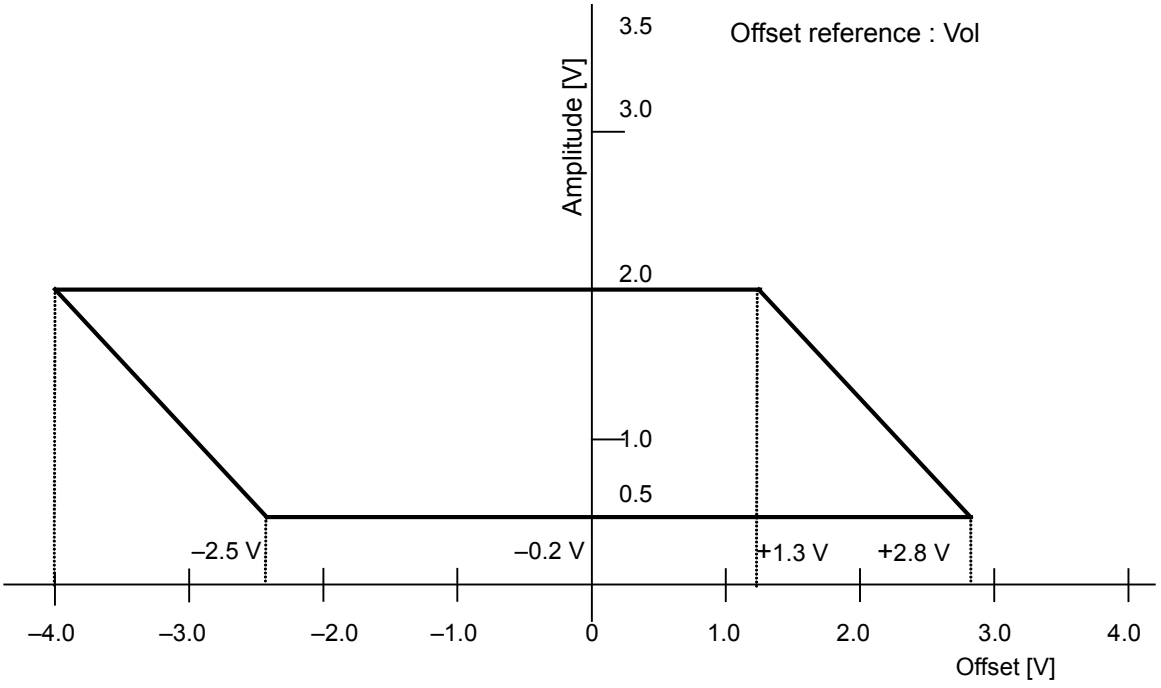


Figure C.2.2-3 MU183020A-x13/x23, MU183021A-x13
Setting range of amplitude and offset based on offset reference (Vol)

C.2.3 Option x13/x23 Data Output (0.5 to 3.5 Vp-p)

Amplitude: 0.5 to 3.5 Vp-p

Offset: –2.0 to +3.3 V (Voh)

(a) When Voh is selected:

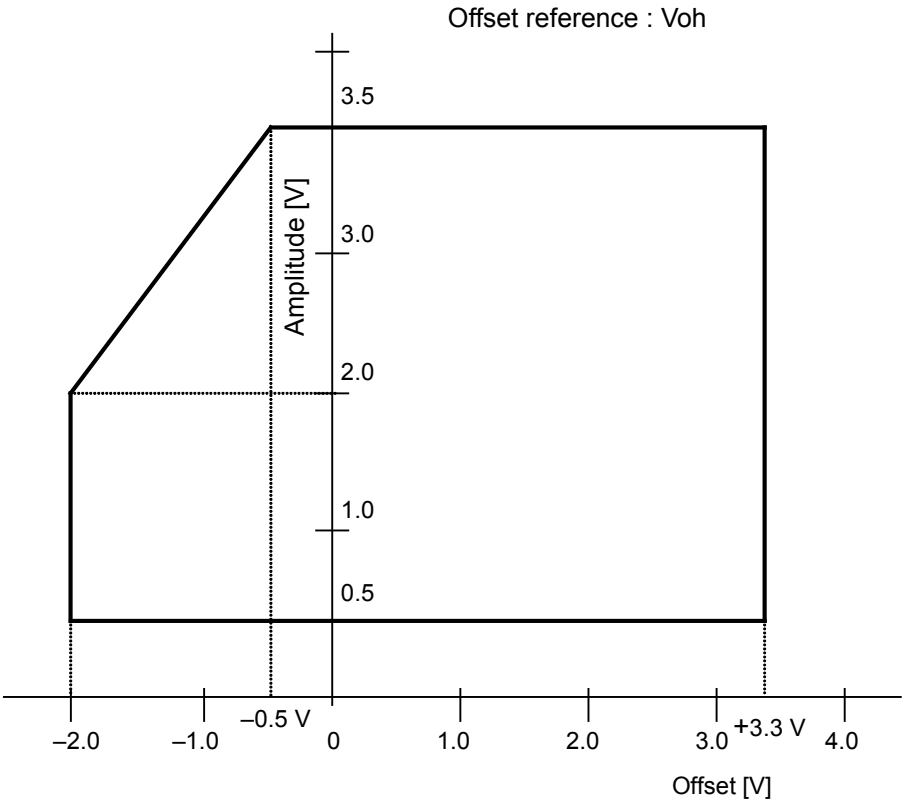


Figure C.2.3-1 MU183020A-x13/x23, MU183021A-x13
Setting range of amplitude and offset based on offset reference (Voh)

(b) When Vth is selected:

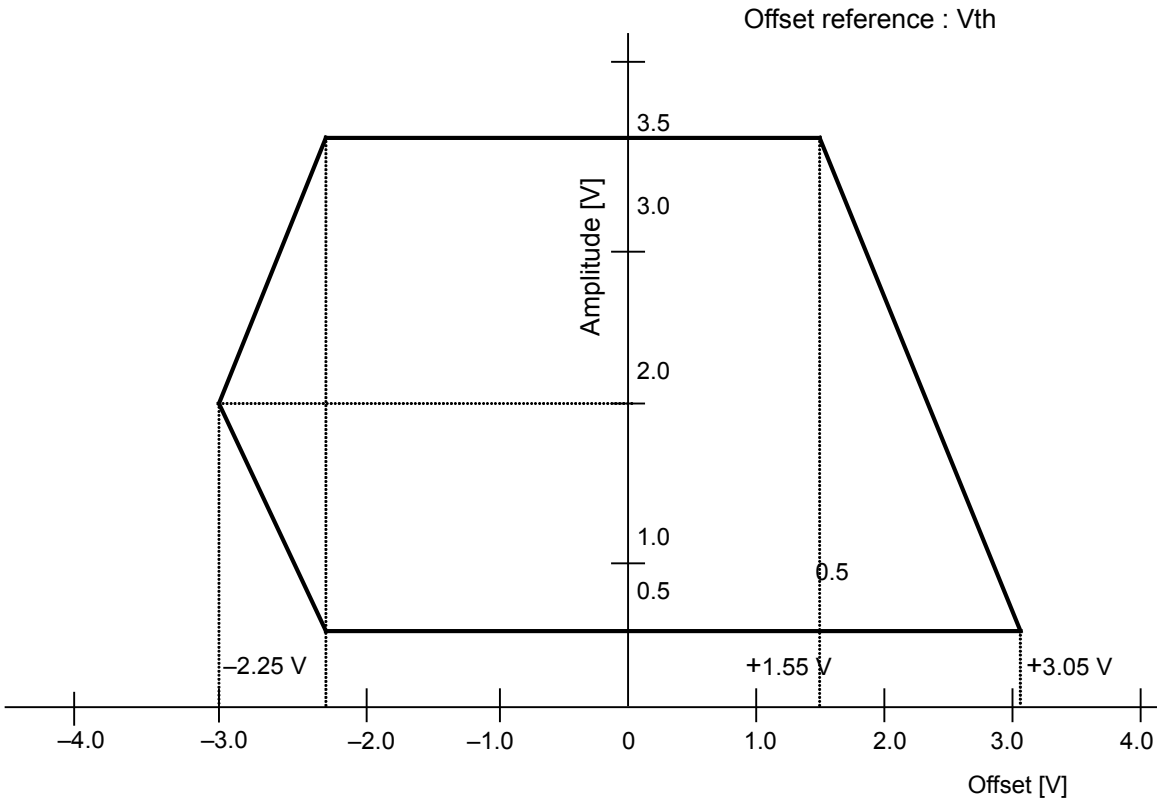


Figure C.2.3-2 MU183020A-x13/x23, MU183021A-x13
Setting range of amplitude and offset based on offset reference (Vth)

(c) When Vol is selected:

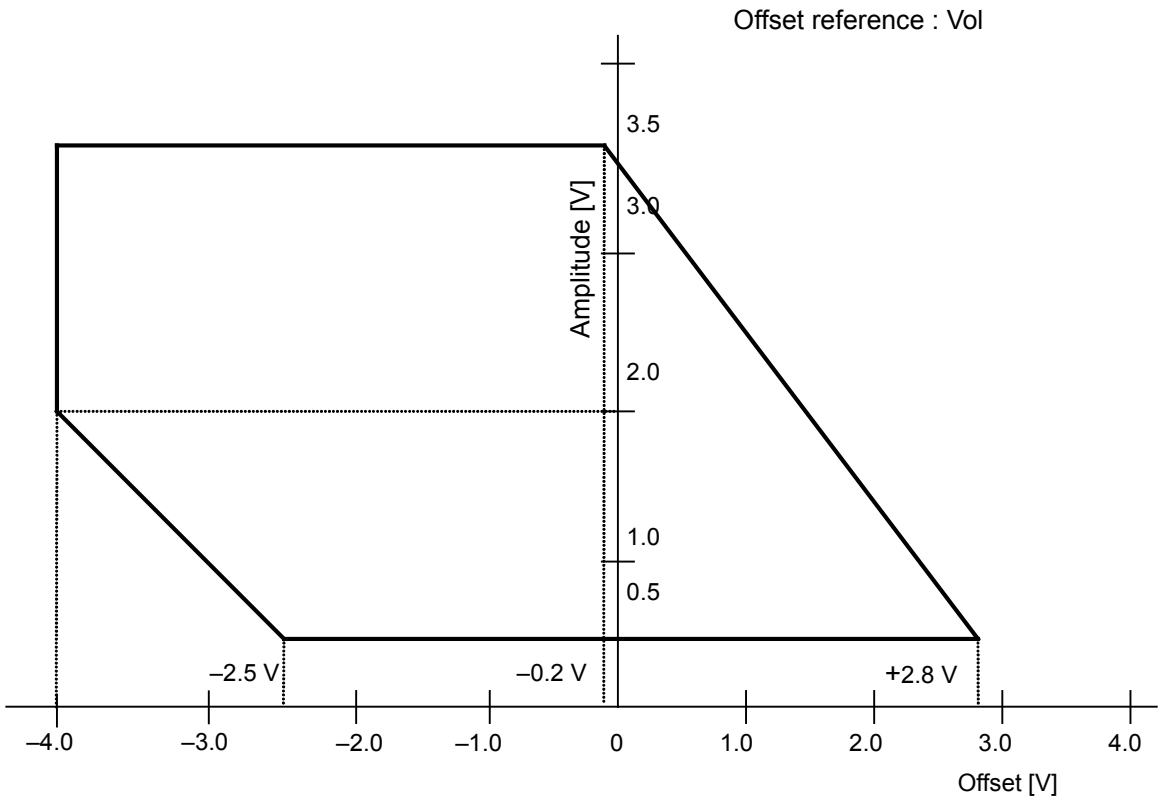


Figure C.2.3-3 MU183020A-x13/x23, MU183021A-x13
Setting range of amplitude and offset based on offset reference (Vol)

C.3 Combination Function Configuration

This section describes the requirements for executing the Combination function by using multiple data interfaces (CH) of MU183020A/MU183021A modules.

All of the following conditions must be satisfied to execute the Combination function.

Enabling conditions for Combination function

- The Module is the MU183020A-x22/x23 or MU183021A.

In addition, the following restriction is added for the Combination function.

Restriction for Combination function

- Combination function cannot set between different modules

C.4 Channel Synchronization Function Configuration

This section describes the requirements for executing the Channel Synchronization function by using multiple data interfaces (CH) of MU183020A/MU183021A modules.

All of the following conditions must be satisfied to execute the Channel Synchronization function.

Enabling conditions for Channel Synchronization function

- Inter-module Channel Synchronization can be set by the following modules.

  MU183020A-x22/x23

  MU183021A
- 2 Channel Synchronization within a module is available to MU183021A.

C.5 Settings Common in Combination System

When the MU183020A/MU183021A is used in a Combination system, some setting items will apply to all the other channels in the Combination system.

Table C.5-1 shows whether the setting items are common or independent in a Combination system.

Table C.5-1 Common/Independent Setting Items in Combination System

Function	Main Category	Sub-Category	Individual Setting Item	Common/ Independent
Output	Data/XData Output ON/OFF			Independent
	Clock Output ON/OFF			Independent
	Amplitude Offset			Independent
	Data/Xdata	Tracking		Independent
		Level Guard		Independent
		Level Guard Setup		Independent
			Amplitude limit	Independent
			Offset limit	Independent
		Defined Interface		Independent
			Amplitude	Independent
			Offset switching	Independent
			Offset	Independent
			External ATT Factor	Independent
		Cross Point		Independent
		Delay		Independent
			Calibration	Independent
			Jitter Input	Common

Table C.5-1 Common/Independent Setting Items in Combination System (Cont'd)

Function	Main Category	Sub-Category	Individual Setting Item	Common/ Independent
Pattern				Common
	PRBS	PRBS Length		Common
		Logic		Common (Pattern Common)
		Mark Ratio		Common (Pattern Common)
	Zero-substit ution	PRBS Length		Common
		Zero Substitution Length		Common
		Additional Bit		Common
	Data	Data Pattern		Common
	Mixed Data	Logic		Common (Pattern Common)
		Block count		Common
		Row Length		Common
		Data Length		Common
		Row count		Common
		PRBS	Pattern	Common
			Mark Ratio	Common (Pattern Common)
		Scramble		Common
		Scramble Setup		Common
		PRBS Sequence		Common
	Pattern Editor	Zoom		Independent
		Block count		Common
		Row Length		Common
		Data Length	Data	Common
			Mixed Data	Common
		Row count		Common

Table C.5-1 Common/Independent Setting Items in Combination System (Cont'd)

Function	Main Category	Sub-Category	Individual Setting Item	Common/ Independent
Error Addition	Error Addition			Common
		Source		Common
		Variation		Common
		Route		Independent
		Error Rate		Common
		When test pattern is Mixed Data: Row 1		Common
Misc1	Pattern Sequence			Common
		Repeat	Pulse Width	Common
			Delay	Common
		Burst	Source	Common
			Data Sequence	Common
			Enable Period	Common
			Burst Cycle	Common
			Delay	Common
			Pulse Width	Common
	Aux Input			Common
	Aux Output			Common
		1/N Clock		Common
		Pattern Sync	For PRBS, Zero Substitution, Data: Position	Common
			For Mixed Data: Block No. Row No.	Common
		Burst Output 2	Delay	Common
			Pulse Width	Common
Misc2	Clock Setting	Clock Source		Common
		Bit Rate		Common
		Output Clock Rate		Common
		Reference Clock		Common
	Combination Setting	Operation method		Common
		Number of channels for Combination		Common
	Grouping Setting	Grouping item setting		Common

Appendix D Performance Test Record Sheet

Document number: _____

Test Location: _____

Date: _____

Test person in charge: _____

Product name: _____

Serial number: _____

Software version: _____

_____

Option: _____

Power voltage: _____ V

Power frequency: _____ Hz

Ambient temperature _____ °C

Relative humidity _____ %

Instruments used: Model name _____ Serial number _____

Model name _____ Serial number _____

Model name _____ Serial number _____

Model name _____ Serial number _____

Remarks _____

_____

_____

D.1 Operating Bit Rate Range

Table D.1-1 MU183020A Operating Bit Rate Range

Option	Clock Source	Operating Bit Rate Rang	Measurement result of BER	Pass/Fail
MU183020A	Internal	2.4 to 28.1 Gbit/s		Pass/Fail
	External	2.4 to 28.1 Gbit/s		Pass/Fail
MU183020A-x01	Internal	2.4 to 32.1 Gbit/s		Pass/Fail
	External	2.4 to 32.1 Gbit/s		Pass/Fail

Table D.1-2 MU183021A Operating Bit Rate Range

Option	Clock Source	Operating Bit Rate Rang	Measurement result of BER	Pass/Fail
MU183021A	Internal	2.4 to 28.1 Gbit/s		Pass/Fail
	External	2.4 to 28.1 Gbit/s		Pass/Fail
MU183021A-x01	Internal	2.4 to 32.1 Gbit/s		Pass/Fail
	External	2.4 to 32.1 Gbit/s		Pass/Fail

D.2 Waveform

Table D.2-1 Data Output

Option	Item	Specification	Result by channel			
			1	2	3	4
MU183020A -x12/x22, MU183021A -x12	Amplitude setting error	0.5 to 2.0 Vp-p, 2 mV Step ±50 mV±17%				
	Offset setting error	–2.0 to +3.3 Voh, 1 mV Step –4.0 Vol Min. ±65 mV ±10% of offset (Vth) ±(Amplitude setting error/2)				
	Tr/Tf	Typ. 25 ps*1,*2,*3				
	Cross Point Adjust	20.0 to 80.0%*3 30.0 to 70.0%*4				
	Jitter	Typ. 8 ps p-p				
MU183020A -x13/x23, MU183021A -x13	Amplitude setting error	0.5 to 3.5 Vp-p, 2 mV Step ±50 mV±17%				
	Offset setting error	–2.0 to +3.3 Voh, 1 mV Step –4.0 Vol Min. ±65 mV±10% of offset(Vth) ±(Amplitude setting error/2)				
	Tr/Tf	Typ. 25 ps*1,*2,*5				
	Cross Point Adjust	20.0 to 80.0%*5 30.0 to 70.0%*4				
	Jitter	Typ. 8 ps p-p				

*1: 20 to 80%

*2: Option x01 is not available: 28.1 Gbit/s

Option x01 is available: 32.1 Gbit/s

*3: Amplitude 2.0 Vp-p

*4: Amplitude 0.998 Vp-p

*5: Amplitude 3.5 Vp-p

Table D.2-2 Clock Output

Option	Item	Specification	Result
Option x01 is not available	Frequency	Full Rate: 2.4 to 28.1 GHz	
		Half Rate: 1.2 to 14.05 GHz	
	Output level	0.3 to 1.0 Vp-p	
MU183020A -x01/ MU183021A -x01	Frequency	Full Rate: 2.4 to 32.1 GHz	
		Half Rate: 1.2 to 16.05 GHz	
	Output level	0.3 to 1.0 Vp-p	

Appendix E Preparing to Use Unit Sync Function

E.1 Preparing to Use Unit Sync Function

This section explains the connections for using the Unit Sync function and the procedure for adjusting the output pattern sync. These examples explain use of four MP1800A main-frame units each containing four MU183020A 2ch PPG modules.

Setup:
Four MP1800A main-frame units
Sixteen MU183020A modules (four modules in each MP1800A)
Channel Synchronization setting
PRBS15 pattern setting

E.1.1 Connections when Using Unit Sync

This section explains the connections for using the Unit Sync function.

Use of the Unit Sync function requires connecting the "Gating Output" connector of the main frame with the "AUX Input" connector. Connect the "Gating Output" and "AUX Input" connectors of each module as described below.
Refer to Section 3.1 "Panel Layout" for the names and functions of connectors.

1. The reference MP1800A is defined as the master unit and the other three are defined as slave units.
2. The "Gating Output" connector of the MU183020A module in Slot 1 of the master MP1800A is connected to the "AUX Input" connector of the same module (Figure E.1.1-1).
3. The "Gating Output" connectors of the MU183020A modules in Slot 2 to Slot 4 of the master MP1800A are connected to the "AUX Input" connectors of the MU183020A modules installed in Slot 1 of each slave MP1800A (Figure E.1.1-1 and Figure E.1.1-2).

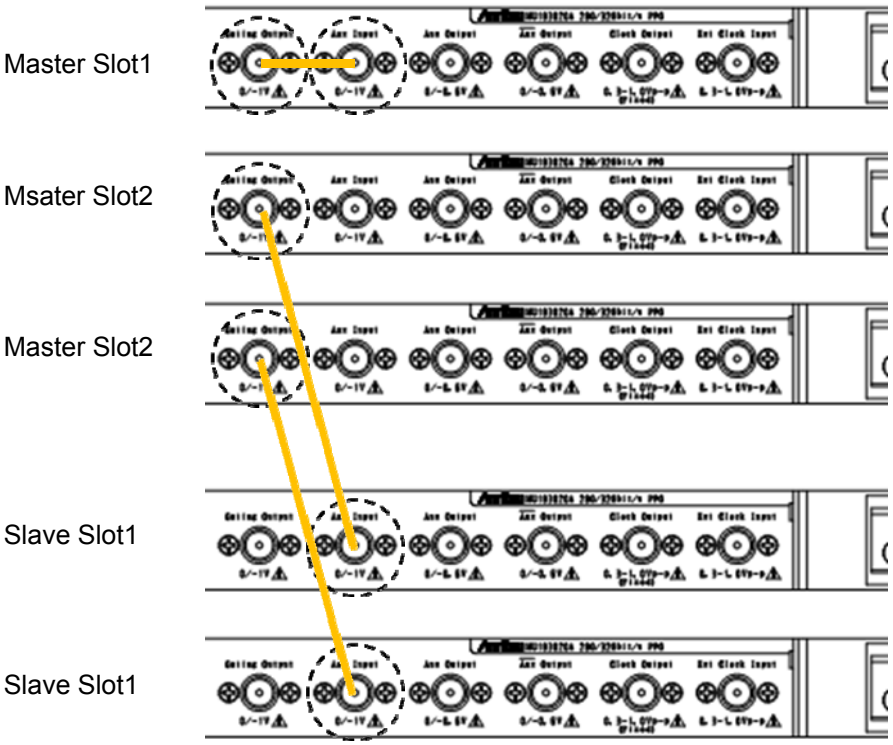


Figure E.1.1-1 MU183020A Connection Examples

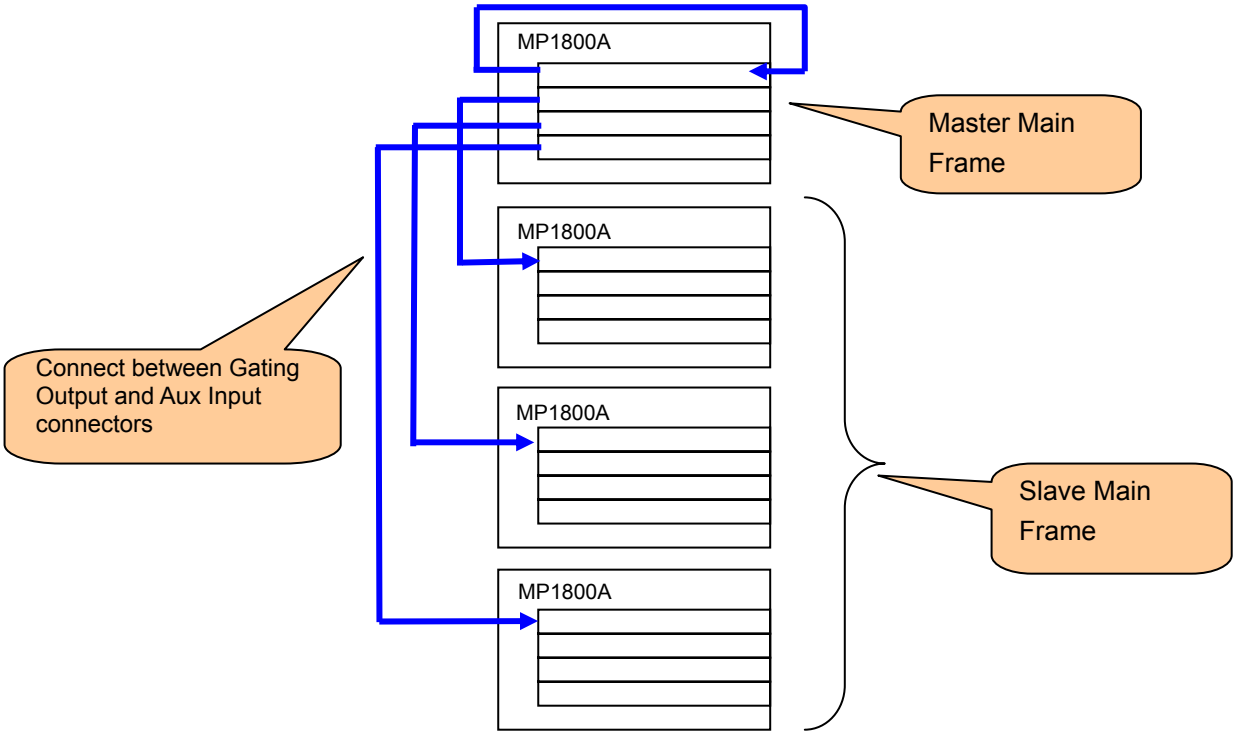


Figure E.1.1-2 Connection Example for Four MP1800A Main Frame Units

E.1.2 Pattern Sync Adjustment Procedure

Use of the Unit Sync functions requires adjustment to compensate for errors caused by differences in the lengths of cables making connections between the main frames and by the specified error (±250 mUI) of the Multi Channel function. After connecting the main frames, set the Unit Sync function to ON and adjust the pattern synchronization between main frames using the following procedure.
Refer to Chapter 5 "Operation Method" for details of each MU183020A setting.

1. Input the clock used by each main frame and module.
   Input a stabilized clock. This adjustment is necessary when the clock input is interrupted or changed.
2. Set the pattern at each main frame or each module.
   Synchronization between main units has an error of ±256 bits. This adjustment requires use of a pattern longer than 513 bits.
   When Unit Sync is set to 2ch Combination or 4ch Combination, the error is a multiple of the number of Combination channels. Set the pattern length as below.
   Pattern length ≥ (512 × N) + 1 bits
   (N = Number of Combination channels)
3. Press **Unit Sync Output** at the master MP1800A.
   If the pattern is changed, it is necessary to synchronize the pattern output by pressing the **Unit Sync Output**.
4. While monitoring the data output of Slot 1 to Slot 4 of each main frame with an oscilloscope, adjust the **Delay** setting at the **Output** tab for each slot to minimize the bit drift. Make this adjustment at all four main frames. Refer to Figure E.1.2-1 and Figure E.1.2-2.
5. Set the signal delay time output from the Gating Output of the MU183020A in Slot 2 to Slot 4 of the master MP1800A using the **Delay** setting at **Pattern Sequence** of the **Misc1** tab for each slot, and then press the **Unit Sync Output**. At this time, adjust the Delay value to minimize the bit drift using while monitoring the data output of Slot 1 of each main frame with an oscilloscope. Refer to Figure E.1.2-3 and Figure E.1.2-4.
6. While monitoring the data of Slot 1 of each main frame with an oscilloscope, use the **Unit Offset** setting of the **Output** tab for any of Slot 1 to Slot 4 of each main frame to minimize the bit drift. Refer to Figure E.1.2-3 and Figure E.1.2-5.

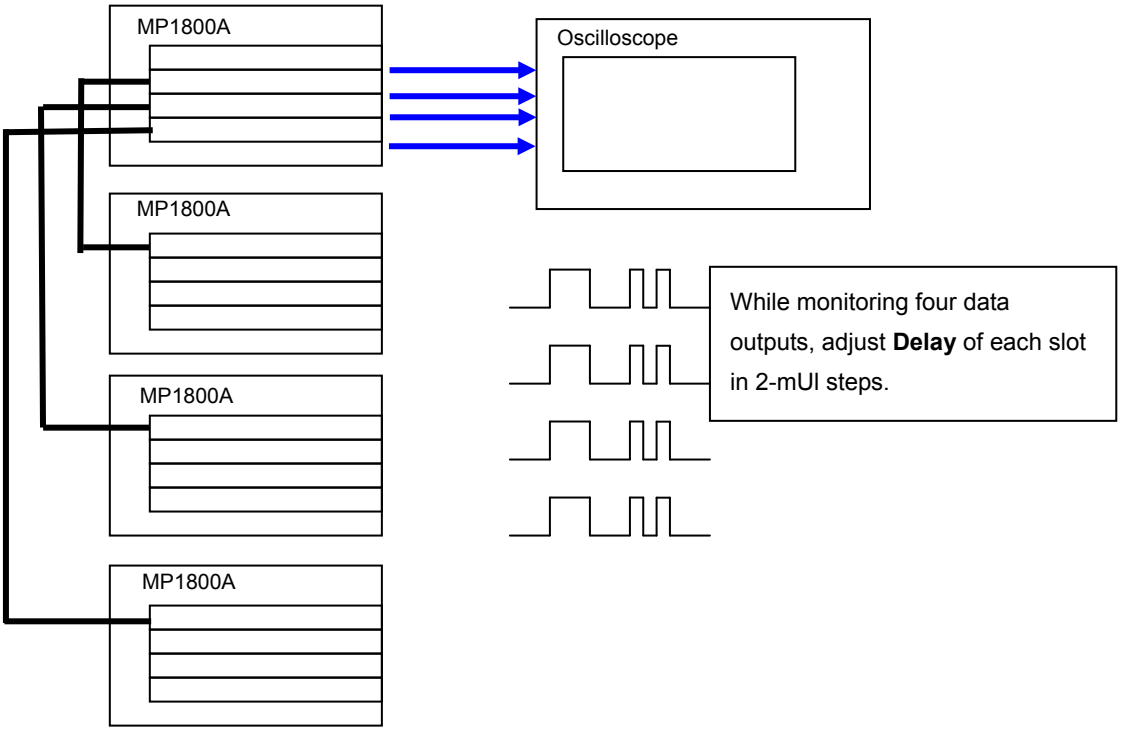


Figure E.1.2-1 Adjusting Output Pattern between Modules

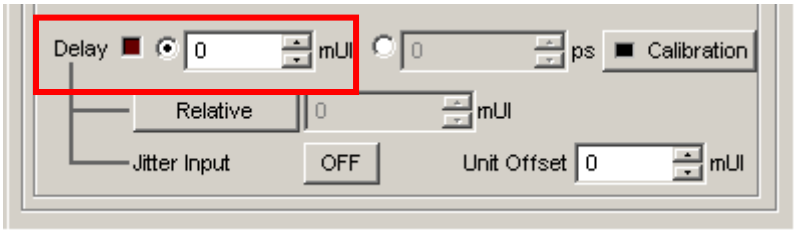


Figure E.1.2-2 Delay Setting Screen

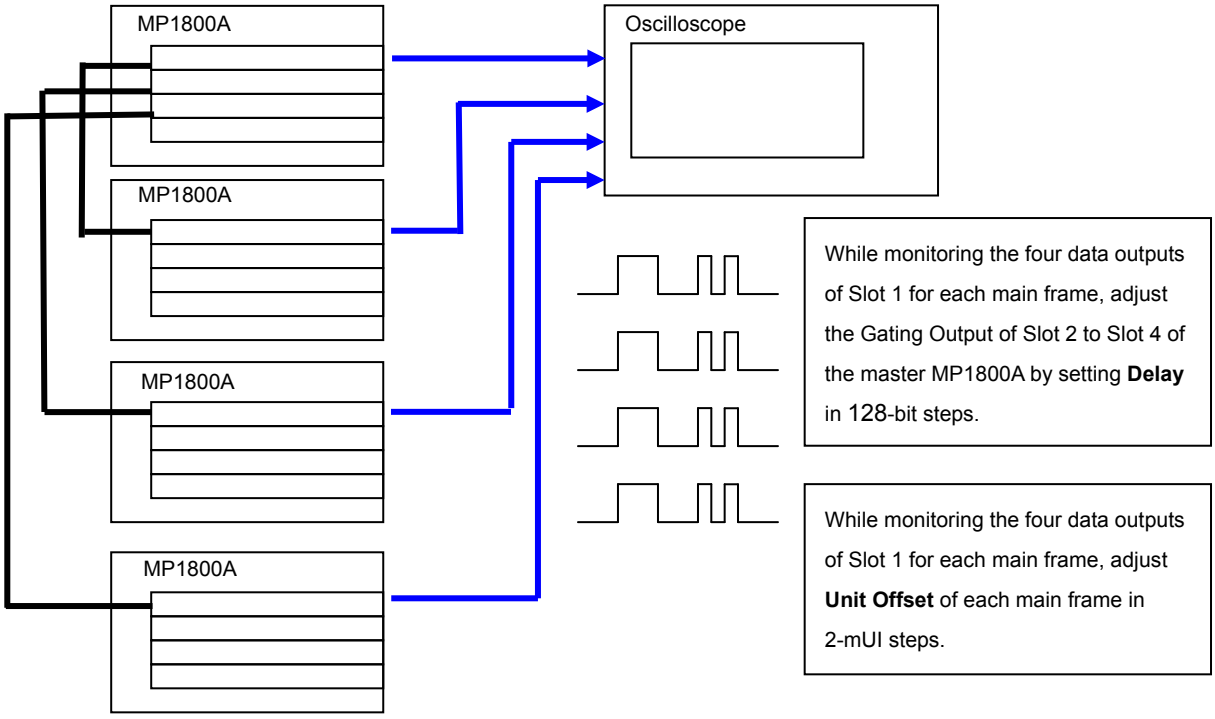


Figure E.1.2-3 Adjusting Output Pattern between Main Units

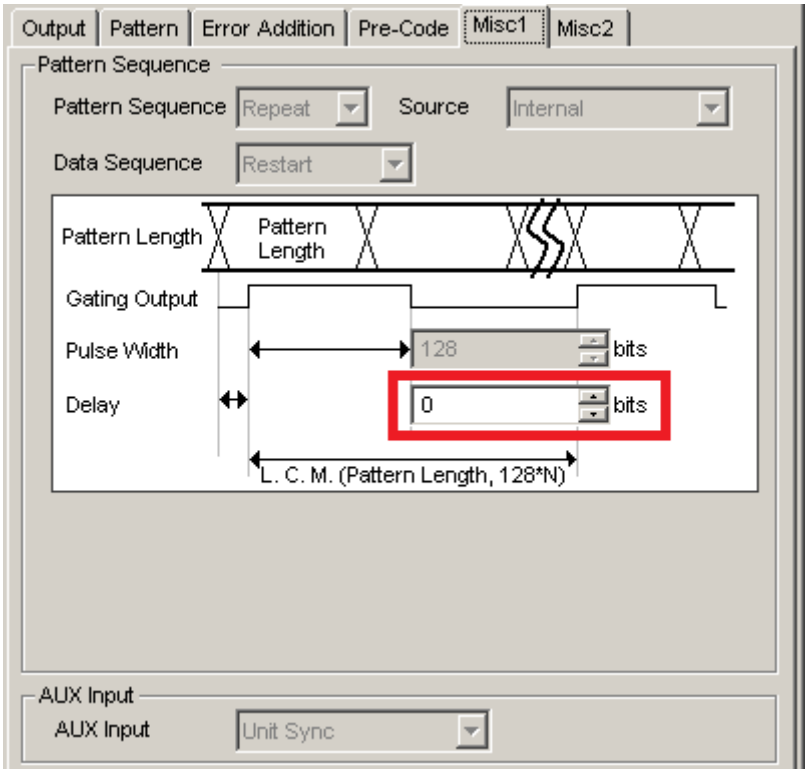


Figure E.1.2-4 Gating Output Delay Setting Screen

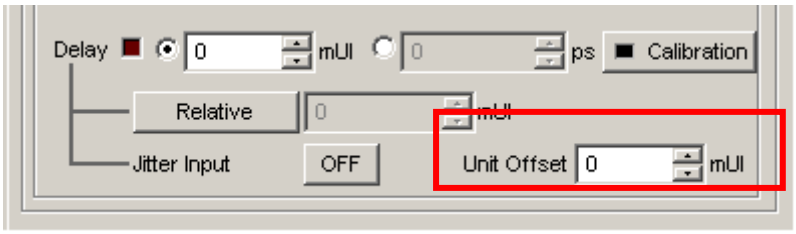


Figure E.1.2-5 Unit Offset Setting Screen

Appendix F Connection Examples for Jitter Measurement

Appendix F describes recommended examples of how to connect MU183020A, MU183040A/B, MU181500B, and/or MP1825B by using applicable coaxial cables. When measurement is performed with jitter added to clock signals by using MU181500B, performance of each instrument is ensured by connecting as described below.

F.1 Jitter-PPG Connection

[Equipment configuration]
MU183020A
MU181500B
DUT

[How to connect instruments, Cable length requirements]

1. Connect a synthesizer and MU181500B's **Ext. Clock Input** connector. The cable length is not especially specified.
2. Connect MU181500B's **Jittered Clock Output** connector and MU183020A's **Ext. Clock Input** connector. The cable length is not especially specified.

3, 4. Use a J1551A coaxial skew match cable (applicable part, pair cable, 0.8 m) to connect MU183020A's **Data Output** and **XData Output** connectors to a DUT.

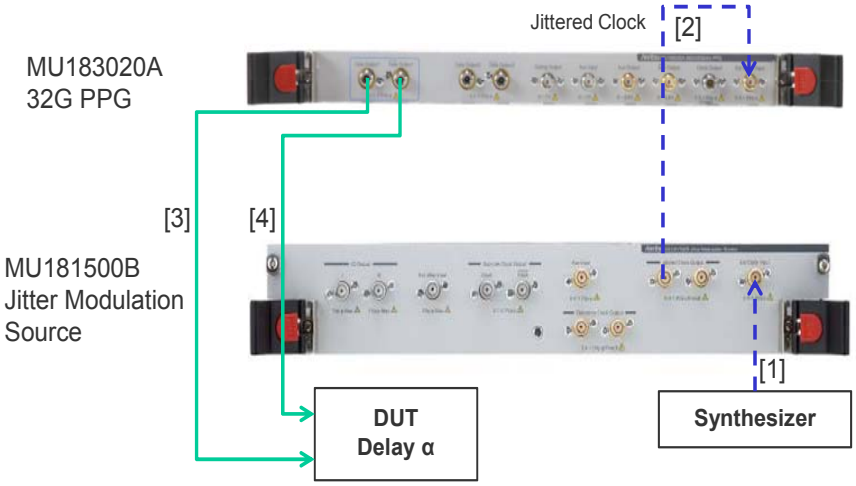


Figure F.1-1 Jitter-PPG Connection Example

F.2 Jitter-PPG-ED Connection

[Equipment configuration]
MU183020A
MU183040B
MU181500B
DUT

[How to connect instruments, Cable length requirements]

1. Connect a synthesizer and MU181500B's **Ext. Clock Input** connector. The cable length is not especially specified.
2. Connect MU181500B's **Jittered Clock Output** connector and MU183020A's **Ext. Clock Input** connector. The cable length is not especially specified.

3, 4. Use a J1551A coaxial skew match cable (Pair cable, 0.8 m) to connect MU183020A's **Data Output** and **XData Output** connectors to a DUT.

5, 6. Use a J1551A coaxial skew match cable (Pair cable, 0.8 m) to connect MU183040B's **Data Input** and **XData Input** connectors to a DUT.

7. Anritsu recommends use of the MU183040B Clock Recovery Option-x22/x23 to supply clock signals to ED. If the option is used, you don't need to connect Cable [7]. If the option is not used, connect the MU183020A's **Clock Output** connector and MU183040B's **Ext. Clock Input** connector with a cable having a length equivalent to the sum of the following:
   - Length of the cable that connects MU183020A's Data Output connector and MU183040B's Data Input connector.
   - Length of the cable that has a length corresponding to a DUT delay amount.
     In the following example, a cable having a length of (1.6m + α) is used to connect the connectors:

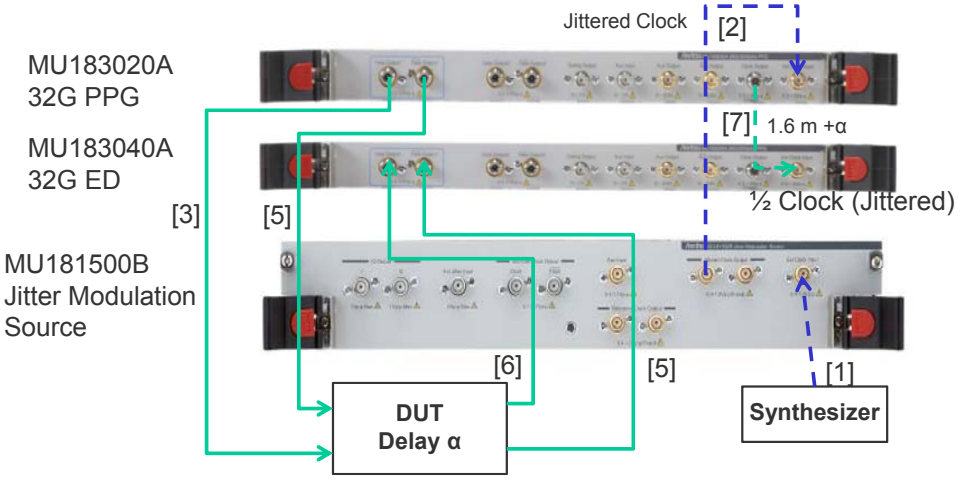


Figure F.2-1 Jitter-PPG-ED Connection Example

F.3 Jitter-PPG-Emphasis Connection

[Equipment configuration]
MU183020A
MU181500B
MP1825B
DUT
J1615A Coaxial Cable Set (Jitter-PPG-Emphasis)

[How to connect instruments, Cable length requirements]

1. Connect a synthesizer and MU181500B's **Ext. Clock Input** connector. The cable length is not especially specified.
2. Connect MU181500B's **Jittered Clock Output** connector and MU183020A's **Ext. Clock Input** connector. The cable length is not especially specified.
3. Use a coaxial cable (applicable part, 0.8 m, K connector) to connect MU183020A's **Data Output** connector and MP1825B's **Data Input** connector.
4. Use a coaxial cable (applicable part, 1.3 m, K connector) to connect MU183020A's **Clock Output** connector and MP1825B's **Clock Input** connector. Then, on the **Misc2** tab of MU183020A, select **Full Rate Clock** in the **Output Clock Rate** box. (Figure F.3-2)

5, 6. Use a J1551A coaxial skew match cable (applicable part, pair cable, 0.8 m) to connect MP1825B's **DataOutput** and **XData Output** connectors to a DUT.

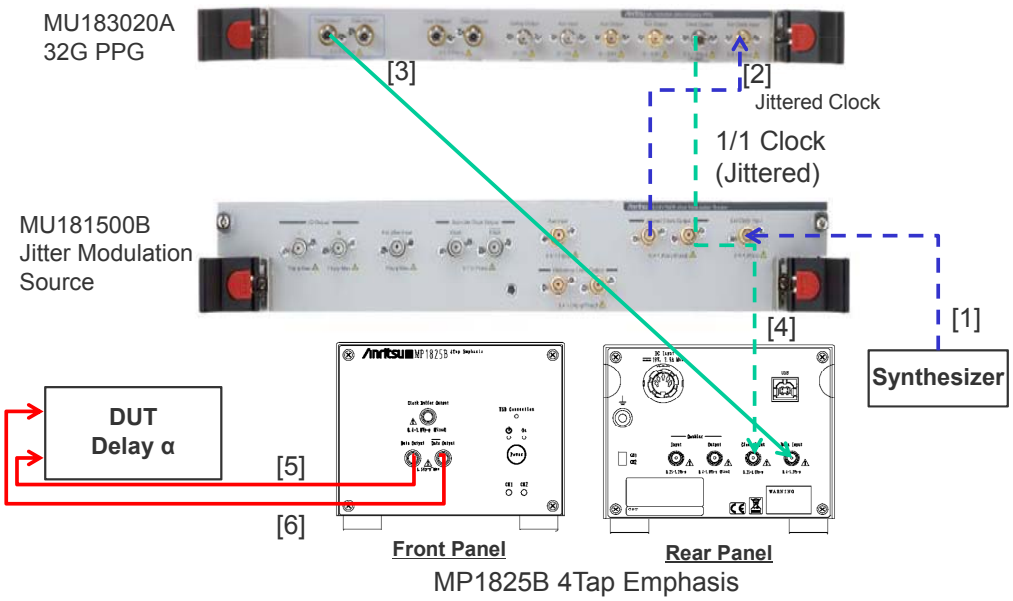


Figure F.3-1 Jitter-PPG-Emphasis Connection Example

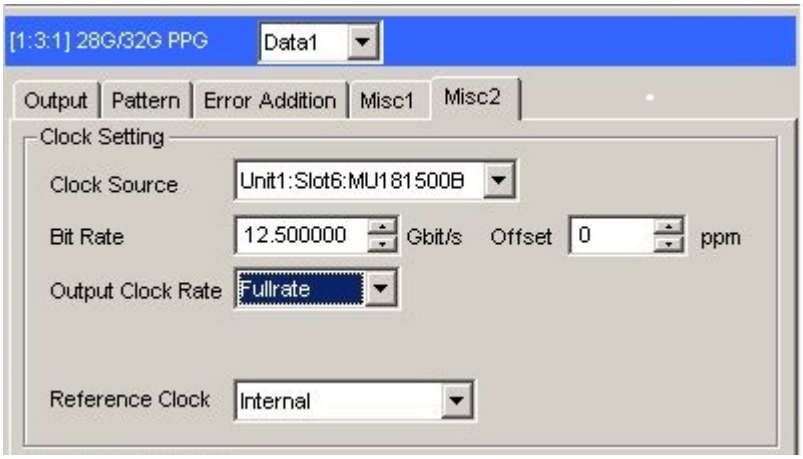


Figure F.3-2 Output Clock Rate Setting on the Misc2 Tab of MU183020A

F.4 Jitter-PPG-Emphasis-ED Connection

[Equipment configuration]
MU183020A
MU183040B
MU181500B
MP1825B
DUT
J1615A Coaxial Cable Set (Jitter-PPG-Emphasis)

[How to connect instruments, Cable length requirements]

1. Connect a synthesizer and MU181500B's **Ext. Clock Input** connector. The cable length is not especially specified.
2. Connect MU181500B's **Jittered Clock Output** connector and MU183020A's **Ext. Clock Input** connector. The cable length is not especially specified.
3. Use a coaxial cable (applicable part, 0.8 m, K connector) to connect MU183020A's **Data Output** connector and MP1825B's **Data Input** connector.
4. Use a coaxial cable (applicable part, 1.3 m, K connector) to connect MU183020A's **Clock Output** connector and MP1825B's **Clock Input** connector. Then, on the **Misc2** tab of MU183020A, select **Fullrate** in the **Output Clock Rate** box. (Figure F.3-2)

5, 6. Use a J1551A coaxial skew match cable (applicable part, pair cable, 0.8 m) to connect MP1825B's **Data Output** and **XData Output** connectors to a DUT.

7, 8. Use a J1551A coaxial skew match cable (applicable part, pair cable, 0.8 m) to connect a DUT with MU183040B's **Data Input** and **XData Input** connectors.

9.10 Anritsu recommends use of the MU183040B Clock Recovery Option-x22/x23 to supply clock signals to ED. If the option is used, you don't need to connect Cables [9] and [10]. If the option is not used, connect MU183020A's **AUX Output** connector and MP1825B's **Doubler Input** connector, and MP1825B's **Doubler Output** connector and MU183040B's **Ext. Clock Input** connector respectively with each cable having a length equivalent to the sum of the following:

- Length of the cable that connects MP1825B's Data Output connector and MU183040B's Data Input connector.
- (Length of the cable that has a length corresponding to DUT delay amount) – 0.5 m.
  In the following example, a cable having a length of (1.6 m – 0.5

m + α) is used. Then, on the Misc1 tab of MU183020A, set the clock rate to 1/4 Clock in the AUX Output area. (Figure F.4-2.)

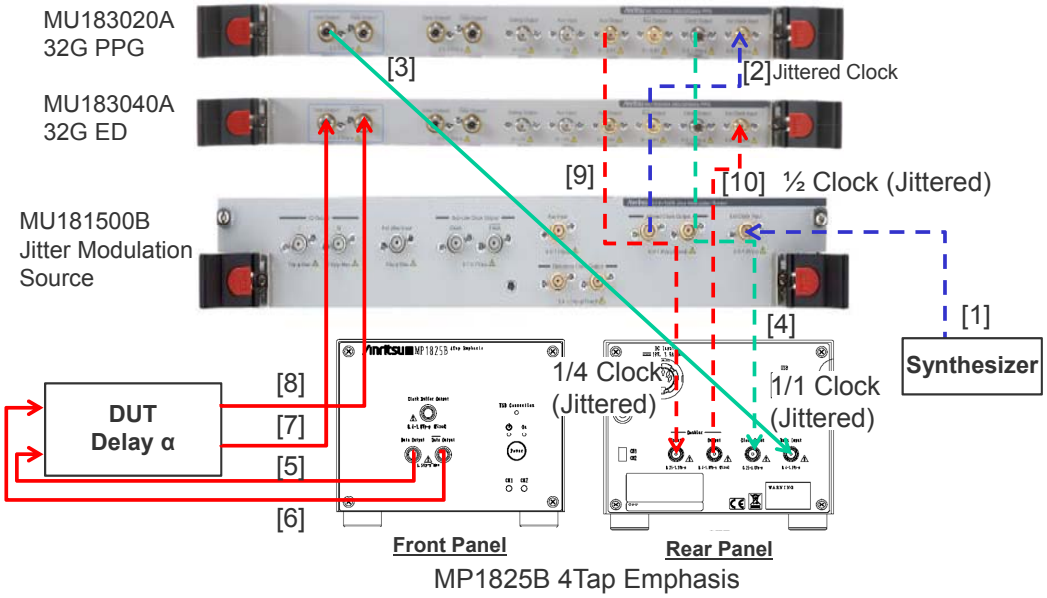


Figure F.4-1 Jitter-PPG-Emphasis-ED Connection Example

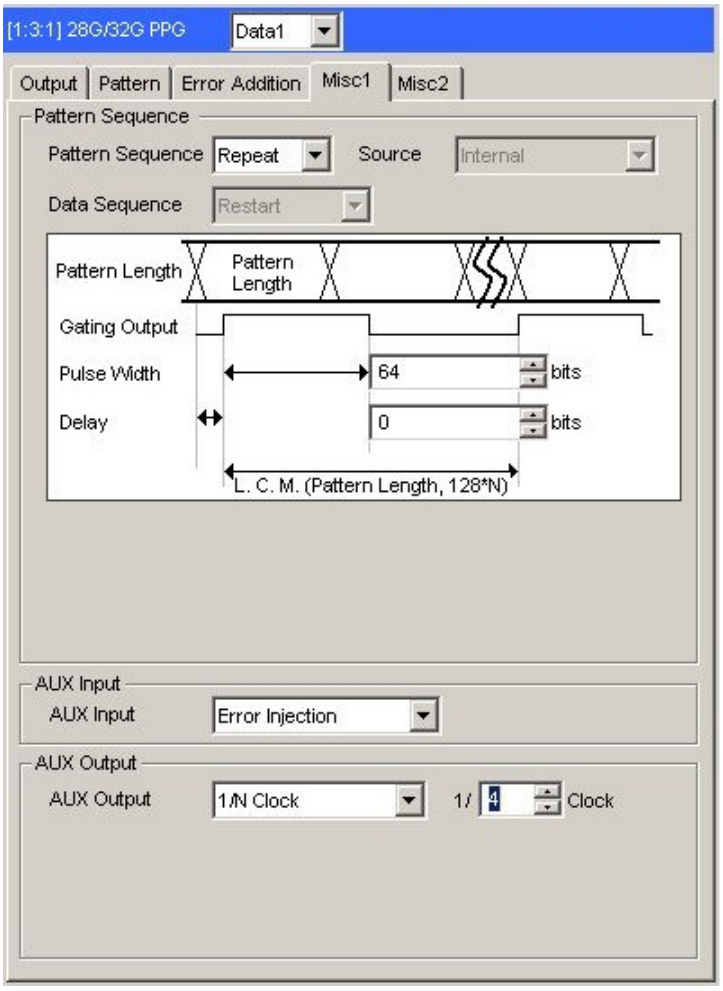


Figure F.4-2 AUX Output Setting on the Misc1 Tab of MU183020A

F.5 Jitter-2ch PPG-Two Emphasis Units Connection

[Equipment configuration]
MU183020A-22/23 2ch PPG
MU181500B
MP1825B-02 (Two units)
DUT
J1618A Coaxial Cable Set (Jitter-2chPPG-Emphasis)

[How to connect instruments, Cable length requirements]

1. Connect a synthesizer and MU181500B's **Ext. Clock Input** connector. The cable length is not especially specified.
2. Use a coaxial cable (applicable part, 0.9 m, K connector) to connect MU181500B's **Jittered Clock Output** connector and MU183020A's **Ext. Clock Input** connector.

3, 4. Use coaxial cables (applicable part, 0.8 m, K connector) to connect MU183020A's **Data Output1** and **Data Output2** connectors respectively with the **Data Input** connector of each MP1825B No.1 and 2. Then, on the **Misc2** tab of MU183020A, select **Halfrate** in the **Output Clock Rate** box. (Figure F.5-2)

5. Use a coaxial cable (applicable part, 0.3 m, APC 3.5mm connector) to connect MU181500B's **Jittered Clock Output** connector and **AUX Input** connector.

6, 7. Use coaxial cables (applicable part, 0.8 m, APC 3.5 mm connector) to connect MU181500B's **Reference Clock Output** connectors respectively with the **Doubler Input** connector of each MP1825B No.1 and 2.Then, connect MP1825B's **Doubler Output** and **Clock Input** connectors with the semi-rigid coaxial cable that comes with MP1825B. After that switch MU181500B's AUX clock input signal to **AUX Input** and set the Reference Clock to **1/1**. (Figure F.5-3)

8, 9. Use J1439A coaxial cables (applicable part, 0.8 m) to connect the **Data Output** connector of each MP1825B No.1 and 2 to a DUT.

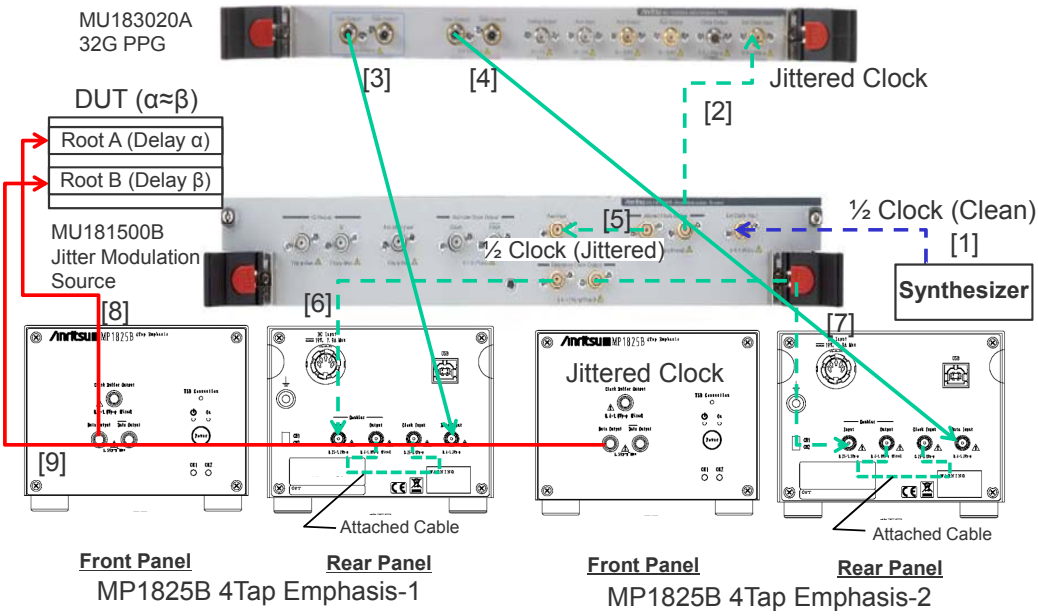


Figure F.5-1 Jitter-2ch PPG-Two Emphasis Units Connection Example

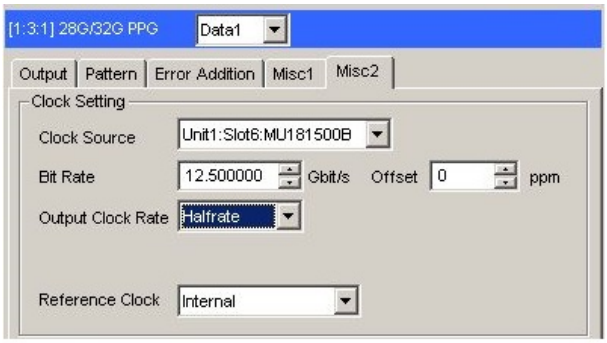


Figure F.5-2 Output Clock Rate Setting on the Misc2 Tab of MU183020A

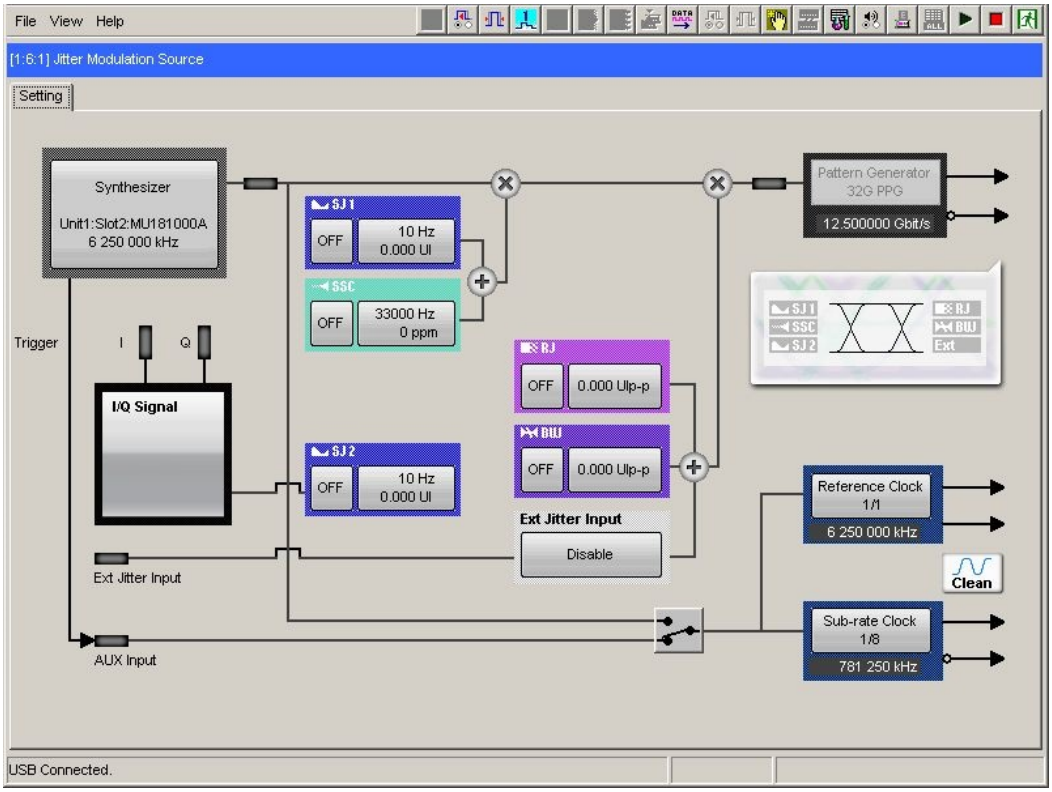


Figure F.5-3 Setting MU181500B's AUX and Reference Clock

F.6 Jitter-2ch PPG-Two Emphasis Units-ED Connection

[Equipment configuration]
MU183020A-22/23 2ch PPG
MU181500B
MP1825B-02 (Two units)
MU183040B-20 2ch ED
DUT
J1618A Coaxial Cable Set (Jitter-2chPPG-Emphasis)

[How to connect instruments, Cable length requirements]

1. Connect a synthesizer and MU181500B's **Ext. Clock Input** connector. The cable length is not especially specified.
2. Use a coaxial cable (applicable part, 0.9 m, K connector) to connect MU181500B's Jittered Clock Output connector and MU183020A's Ext. Clock Input connector.

3, 4. Use coaxial cables (applicable part, 0.8 m, K connector) to connect MU183020A's **Data Output1** and **Data Output2** connectors respectively with the **Data Input** connector of each MP1825B No.1 and 2. Then, on the **Misc2** tab of MU183020A, select **Halfrate** in the **Output Clock Rate** box. (Figure F.5-2)

5. Use a coaxial cable (applicable part, 0.3 m, APC 3.5mm connector) to connect MU181500B's **Jittered Clock Output** connector and **AUX Input** connector.

6, 7. Use coaxial cables (applicable part, 0.8 m, APC 3.5 mm connector) to connect MU181500B's **Reference Clock Output** connectors respectively with the **Doubler Input** connector of each MP1825B No.1 and 2. Then, connect MP1825B's **Doubler Output** and **Clock Input** connectors with the semi-rigid coaxial cable that comes with MP1825B. After that switch MU181500B's AUX clock input signal to **AUX Input** and set the Reference Clock to **1/1**. (Figure F.5-3)

8, 9. Use J1439A coaxial cables (applicable part, 0.8 m) to connect the **Data Output** connector of each MP1825B No.1 and 2 to a DUT.

10, 11. Use J1439A coaxial cables (applicable part, 0.8 m) to connect a DUT with MU183040B's **Data Input1** and **Data Input2** connectors.

12. Anritsu recommends use of the MU183040B Clock Recovery Option-x22/x23 to supply clock signals to ED. If the option is used, you don't need to connect Cable [12]. If the option is not used, connect the MP1825B's **Clock Buffer Output** connector and MU183040B's **Ext. Clock Input** connector with a cable having a length equivalent to the sum of the following:

- Length of the cable that connects MP1825B's Data Output connector and MU183040B's Data Input connector.
- (Length of the cable that has a length corresponding to DUT delay amount (α ≈ β)) + 0.5 m.
  In the following example, a cable having a length of (1.6 m + 0.5 m + α) is used.

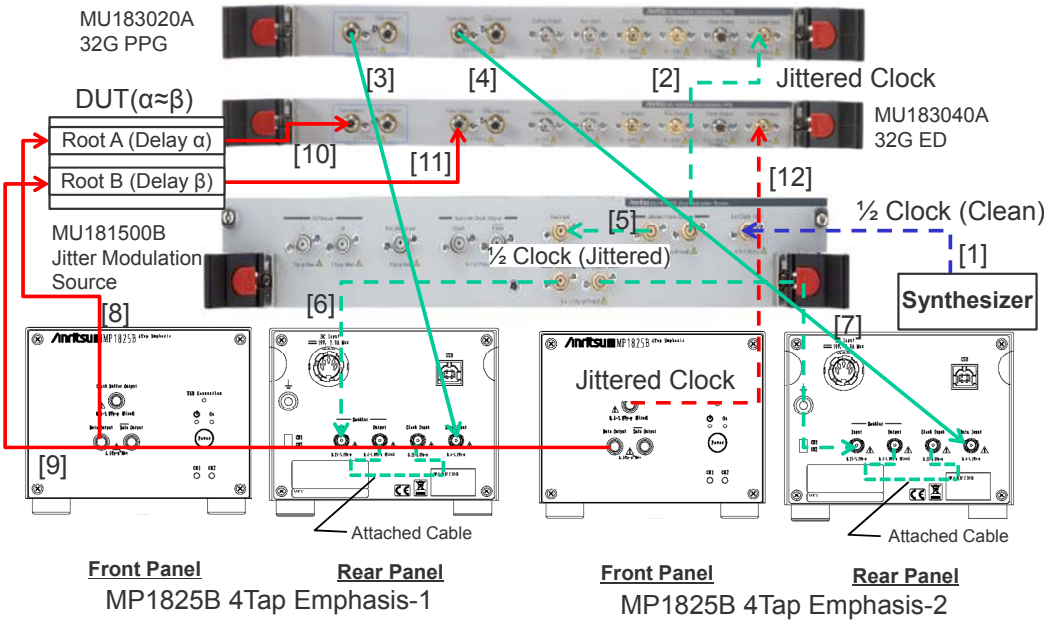


Figure F.6-1 Jitter-2ch PPG-Two Emphasis Units-ED Connection Example

Appendix G How to Use PAM Function

This section explains how to use the PAM (Pulse Amplitude Modulation) function.

G.1 BER Measurement of PAM Signal

This section explains PAM4 signal generation and BER measurement. In the example here, the MU183020A 32G 2ch PPG and the MZ1834B 4PAM Converter are used to generate PAM signal, and the MU183040B 32G High Sensitivity ED is used for BER measurement of PAM signal.

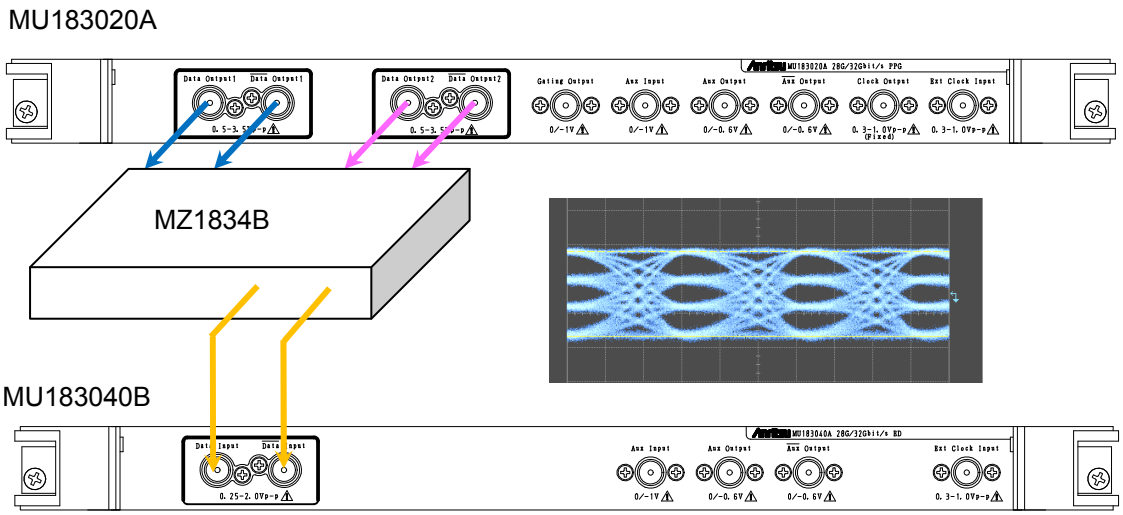


Figure G.1-1 PAM Signal and Connection Example for BER Measurement

Figure G.1-2 shows PAM4 signals generated in PPG1 and PPG2 patterns. 32G PPG Data output is PPG1, Data2 output is PPG2, and MZ1834B output is PAM4.
Threshold1 to Threshold3 on the left side of the PAM4 waveform are the threshold voltages to judge PAM4 amplitude values. For PAM4 has four values, three different threshold voltages, Threshold1 to 3, are required to distinguish each voltage value. The 32G ED measures the BER of these three threshold values.
When using one ED, perform BER measurement three times changing the threshold voltage from Threshold1 to Threshold3.
If divide and input PAM4 signals into three EDs, the BER can be measured at only one time by setting values of Threshold1 to 3 for the three EDs respectively.

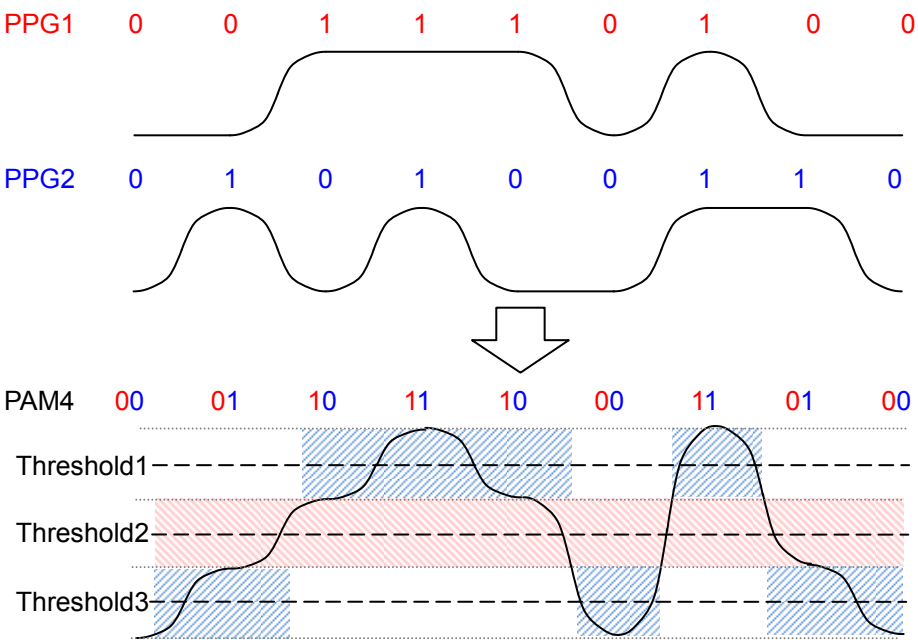


Figure G.1-2 PAM Signals and Thresholds at BER Measurement

The Threshold2 pattern is the same as the PPG1 pattern. The PPG2 pattern appears half in the Threshold1 area and half in the Threshold3 area.

The PPG2 pattern is marked with blue shaded areas in Figure G.1-2. The PPG2 pattern appears in the Threshold3 area when Threshold2 is 0 (low) and in the Threshold1 area when Threshold2 is 1 (high).

Because the data patterns for Threshold1 and 3 are generated from one PPG and divided into two, the BER measured by these thresholds is incorrect. However, when patterns expected for each threshold are already known, the BER of PAM signal can be measured by setting the patterns on the ED.

For details of PAM signal generation, refer to the Application Note entitled "PAM (Pulse Amplitude Modulation)Signal Generation for QAM Transmission".

G.2 Setting PPG

This section explains how to set PPG when generating PAM waveform.

1. Click the **Misc2** tab.
2. Click the **Setting...** button.

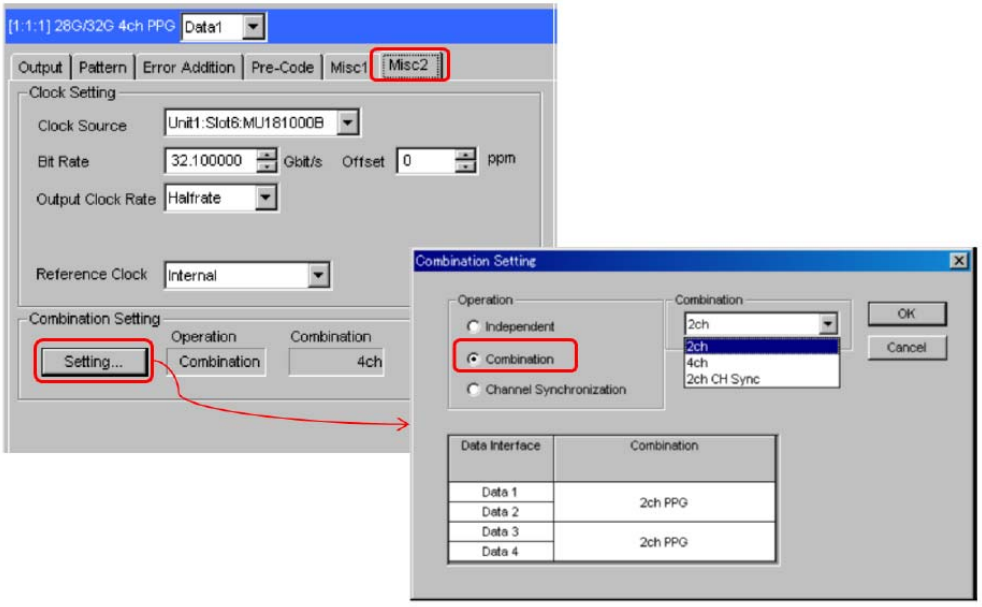


Figure G.2-1 Combination Setting

3. Check **Combination** and select **2ch**.

Table G.2-1 PPG Setting for Pattern

Pattern	Combination Settings	Pattern File for PPG1 and PPG2
PRBS7	Operation: Combination Combination: 2ch	No file. Test Pattern [PRBS] is used.
PRBS9		
PRBS10		
PRBS11		
PRBS15		
PRBS20		
PRBS23		
PRBS13Q		PRBS13Q.txt
GrayPRBS13Q		GrayPRBS13Q.txt
PRQS10		PRQS10.txt
SSPR		SSPR.txt
JP03A		JP03A.txt
JP03B		JP03B.txt
Squarewave		Squarewave.txt

4. Click the **Pattern** tab. Setting a pattern varies according to a PAM pattern generated.
5. Set **Test Pattern** as follows.
   - For PRBS7 to PRBS23, select **PRBS** and set **Length**.
   - For PRBS13Q to Squarewave, select **Data** and click **Edit**. Load a pattern file from the File menu on the Pattern Editor dialog box in Figure G.2-3.

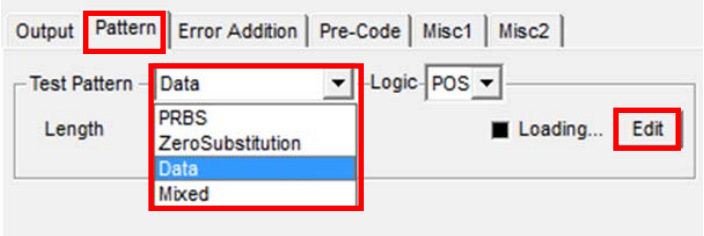


Figure G.2-2 Pattern Setting

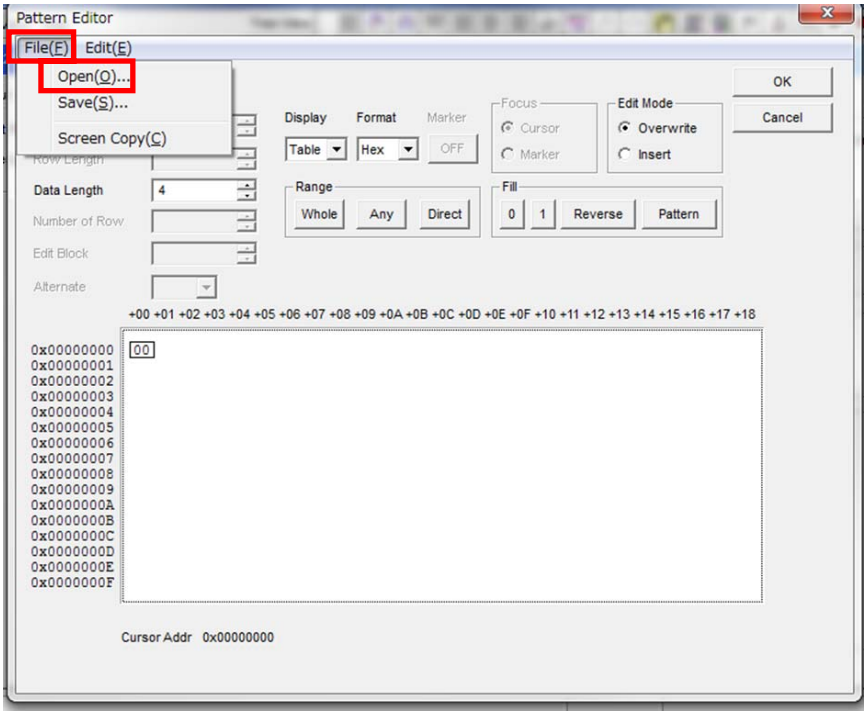


Figure G.2-3 Pattern Editor File Menu

Setting Examples

- To set PRBS15:

1. Click **Settings…** on the **Misc2** tab.
2. On the **Combination Setting** dialog box, select **Combination** and **2ch**.
3. Select **PRBS** from the **Test Pattern** pull down menu.
4. Set **Length** to **2^15-1**.

- To set PRBS13Q:

1. Click **Settings…** on the **Misc2** tab.
2. Select **Combination** on the Combination Setting dialog box, and select **2ch**.
3. Click the **Pattern** tab of Data1.
4. Select **Data** from the **Test Pattern** pull down menu.
5. Click **Edit**.
6. Click **File** > **Open**.
7. Click PRBS13Q.txt in the \Pattern Files\PAM_Pattern\PRBS13Q folder.

G.3 Setting ED

This section explains how to set the ED when executing BER measurement of PAM waveform.
As explained in G.1 "BER Measurement of PAM Signal", an ED pattern should be changed for Threshold1 to Threshold 3 individually.
For the ED screen operation, refer to 5.14 "PAM BER Measurement" in the *MU183040A 28G/32G bit/s ED MU183041A 28G/32G bit/s 4ch ED MU183040B 28G/32G bit/s High Sensitivity ED MU183041B 28G/32G bit/s 4ch High Sensitivity ED Operation Manual*.

1. Click the **Misc2** tab of the ED.
2. Click the **Setting…** button.
3. Click **Independent**.
4. Click the **Pattern** tab. How to set a pattern varies according to a threshold type and a PAM pattern to measure.
   - To set Threshold2 pattern to PRBS7 to PRBS23:
     Select **PRBS** and set **Length**.
   - Other cases:

     Select **Data** and click **Edit**.

     Load a pattern file from the File menu on the Pattern Editor dialog box in Figure G.2-3.

Table G.3-1 ED Setting According to Threshold Type/Pattern

Pattern Type	Pattern for Threshold1	Pattern for Threshold2	Pattern for Threshold3
PRBS7	PRBS7_Upper_bin.txt	No file. Test Pattern [PRBS] is used.	PRBS7_Lower_bin.txt
PRBS9	PRBS9_Upper_bin.txt		PRBS9_Lower_bin.txt
PRBS10	PRBS10_Upper_bin.txt		PRBS10_Lower_bin.txt
PRBS11	PRBS11_Upper_bin.txt		PRBS11_Lower_bin.txt
PRBS15	PRBS15_Upper_bin.txt		PRBS15_Lower_bin.txt
PRBS20	PRBS20_Upper_bin.txt		PRBS20_Lower_bin.txt
PRBS23*	PRBS23_Upper_bin.txt		PRBS23_Lower_bin.txt
PRBS13Q	PRBS13Q_Upper.txt	PRBS13Q_Middle.txt	PRBS13Q_Lower.txt
GrayPRBS13Q	GrayPRBS13Q_Upper.txt	GrayPRBS13Q_Middle.txt	GraeyPRBS13Q_Lower.txt
PRQS10	PRQS10_Upper.txt	PRQS10_Middle.txt	PRQS10_Lower.txt
SSPR	SSPR_Upper.txt	SSPR_Middle.txt	SSPR_Lower.txt
JP03A	JP03A_RX.txt		
JP03B	JP03B_RX.txt		
Squarewave	Squarewave_RX.txt		

*: The BER value cannot be measured correctly due to the limits of the Block Window function. The error count of each Threshold 1 and Threshold 3 will be greater than the expected value because the

Block Window does not mask some of the bits that are not objects of measurement.

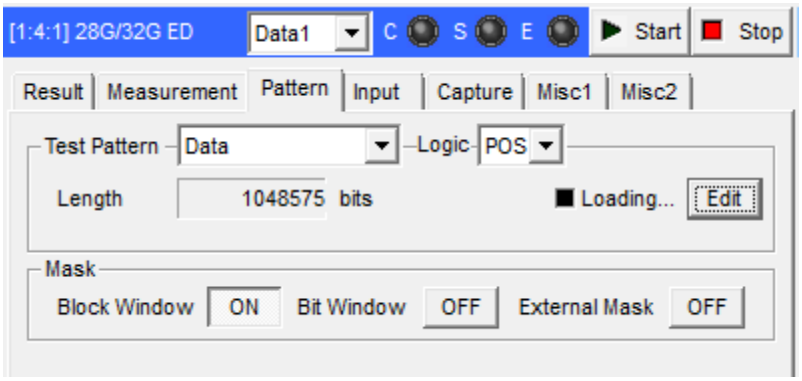


Figure G.3-1 Setting Pattern

5. Click the **Block Window** button to turn it **ON**.

Setting Examples

- To measure BER of PRBS15 at Threshold1:

1. Clik **Settings…** on the **Misc2** tab.
2. Select **Independent**.
3. Click the **Pattern** tab.
4. Select **Data** from the **Test Pattern** pull down menu.
5. Click **Edit**.
6. Click **File** > **Open** on the Pattern Editor dialog box.
7. Select PN15_Upper_bin.txt in the \Pattern Files\PAM_Pattern\PRBS15 folder.
8. Click **OK**.
9. Click the **Block Window** button to turn it **ON**.

- To measure BER of PRBS15 at Threshold2:

1. Click **Settings…** on the **Misc2** tab.
2. Select **Independent**.
3. Click the **Pattern** tab.
4. Select **PRBS** for **Test Pattern**.
5. Set **Length** to **2^15-1**.

- To measure BER of PRBS13Q at Threshold3:

1. Click **Settings…** on the **Misc2** tab.
2. Select **Independent**.
3. Click the **Pattern** tab.
4. Select **Data** from the **Test Pattern** pull down menu.
5. Click **Edit**.
6. Click **File** > **Open** on the **Pattern Editor** dialog box.
7. Select PRBS13Q_Lower.txt in the \Pattern Files\PAM_Pattern\PRBS13Q folder.
8. Click **OK**.
9. Click the **Block Window** button to turn it **ON**.